

Algerian People's Democratic Republic Ministry of Higher Education and Scientific Research Ecole Nationale Polytechnique Département d'Electronique Laboratoire des Dispositifs de Communication et de Conversion Photovoltaïque



PhD Thesis

ELECTRONIC Presented by: LOUKRIZ Abdelhamid Master in Electronics, University of Msila

<u>Theme</u>

Implementation of photovoltaic inverter

controller on DSP

The defense expected: 17/10/2016, the Board of Examiners composed of:

M.LARBES Cherif M. HADDADI Mourad M.MALEK Ali M.TALHA Abdelaziz M.BOUSBIA SALAH Hicham M.OUADAH Abderahim

Professor ,ENP Professor ,ENP Researches Director,CDER Professor ,USTHB Lecturer A, ENP General manager MIE President Supervisor Examiner Examiner Guest



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Table of contents

List of Figures	
List of Tables	
General introduction	09
I. The PV systems and the smart grids	
Introduction	13
1-1 Introduction in the Photovoltaic systems	14
1-2 Photovoltaic characteristics.	15
1.2.1 Effect Temperature on Voc	15
1.2.2 Effect Irradiance on Ics	16
1.2.3 Maximum Tracking Point (MPPT)	17
1.3 Types of PV systems	17
1.3.1 Stand-Alone PV system	18
1.3.2 Grid-Tied PV system	18
1.3.3 Hybrid systems	19
1.4 Vision for future electricity systems	20
1.4.1 Advanced Grid Features	22
1.4.2 Communication	23
1.4.3 Future-proof	
1.5 PV inverters and Smart Grid	24
1.6 Topologies of Grid Connected PV systems	25
1.6.1 Centralized inverters	25
1.6.2 String Inverters	26
1.6.3 Multi-String inverters	27
1-7 International Codes and Standards for Grid Connected PV system	
Conclusion	
II. Design of the PV-Inverter	
Introduction	31
2.1 Design of Input LC Filter	32
2.1.1 Input Inductance (L_{PV})	32
2.1.2 Input capacitance (C _{PV})	

2.2 Design of Flyback Converter	33	
2.2.1 Original of the flyback converter	33	
2.2.2 Flyback Modes of Operation: DCM vs CCM	35	
2.2.3 Designing the power stage of flyback converter		
2.3 Design of H-bridge inverter	45	
2.3.1 Theory of operation	46	
2.3.2 Calculation of DC-link Capacitor	46	
2.3.2.1 Electrolytic Capacitors vs Film Capacitors	47	
2.3.1.2 Sizing the DC-link Capacitor	48	
2.3.3 Switching Circuit Configuration	49	
2.3.4 Driver and isolation Switching Circuit	49	
2.3.4 .1 Determining bootstrap capacitance, CB-STRAP	50	
2.3.4 .2 Determining bootstrap diode, DBS, and resistor, RC	52	
2.4 Design of output Filter	53	
2.5 Components for the implementation	55	
Conclusion	56	

III. Controller of the PV-Inverter

Introduction	
3 .1 Control of Flyback converter	
3.1.1 Maximum Power Point Tracker (MPPT)	60
3.1.1.1 Perturb and Observe method	61
3.1.1.2 Incremental Conductance method	
3.1.1.3 Parasitic Capacitance method	63
3.1.1.4 Constant Voltage method	64
3.1.1.5 Constant Current method	64
3.1.2 Proposed Algorithm Variable Step Size IC MPPT (VSS IC)	64
3 .2 Control of H-bridge Inverter	70
3.2.1 DC-Link Controller	70
3.2.2 Grid Synchronization and current control	74

3.2.3.1 Sinusoidal pulse width modulation (SPWM)	74
3.2.3.2 SPWM with bipolar voltage switching	75
3.2.3.3 SPWM with unipolar voltage switching	76
Conclusion	
IV. Simulation and experimental validation for Grid connected PV- inverter	
Introduction	81
4.1 Simulation results for Grid connected PV inverter	82
4.1.1 Flyback and new IC variable step size MPPT algorithm simulation	84
4.1.1.1 MPPT tracking	84
4.1.1.2 Response time	85
4.1.1.3 Duty cycle oscillations	86
4.1.1.4 Ripple	86
4.1.1.5 Overshoot	87
4.1.2 H-bridge Inverter simulation testing	
4.1.2.1 H-bridge autonomy Inverter simulation	88
4.1.2.2 Grid connected H-bridge inverter simulation	90
4.2 Experimental results for Grid connected PV inverter	92
4.2.1 Experimental results of the proposed variable step size IC MPPT	93
4.2.2 Experimental results of H-bridge inverter	86
Conclusion	99
General conclusion and future research	100
Appendix	101
References	108

List of Figures

	13
Fig.1.2 I-V characteristics of a PV module with temperature variation	14
Fig.1.3 I-V characteristics of a PV module with irradiance variation	15
Fig.1.4 Voltage and Power characteristics of a PV module	16
Fig.1.5 Stand-Alone Photovoltaic System	17
Fig.1.6 Grid-Tied Photovoltaic System	18
Fig.1.7 Schematic representation of a hybrid system	19
Fig.1.8 Conception of Smart grid network	20
Fig.1.9 Historic of Smarter electricity systems	21
Fig.1.10 PV Central Inverters	22
Fig.1.11 String Inverters	26
Fig.1.12 Multi-String Inverters	27
Fig.1.13 Module inverters	27
Fig.2.1 Basic diagram of PV inverter	27
Fig.2.2 Derivation of the flyback converter	
Fig.2.3 Flyback Schematic	
Fig.2.4 CCM and DCM Flyback Current Waveforms	
Fig.2.4 CCM and DCM Flyback Current Waveforms Fig.2.5 Flyback converter circuit configuration	
Fig.2.4 CCM and DCM Flyback Current WaveformsFig.2.5 Flyback converter circuit configurationFig.2.6 Flyback converter with primary RC snubber.	
 Fig.2.4 CCM and DCM Flyback Current Waveforms Fig.2.5 Flyback converter circuit configuration Fig.2.6 Flyback converter with primary RC snubber. Fig.2.7 General design of H-bridge inverter. 	
 Fig.2.4 CCM and DCM Flyback Current Waveforms Fig.2.5 Flyback converter circuit configuration Fig.2.6 Flyback converter with primary RC snubber Fig.2.7 General design of H-bridge inverter. Fig.2.8 Generic DC-link voltage waveform 	
 Fig.2.4 CCM and DCM Flyback Current Waveforms Fig.2.5 Flyback converter circuit configuration Fig.2.6 Flyback converter with primary RC snubber. Fig.2.7 General design of H-bridge inverter. Fig.2.8 Generic DC-link voltage waveform. Fig.2.9 Bootstrap Driver Mosfet circuit. 	
 Fig.2.4 CCM and DCM Flyback Current Waveforms Fig.2.5 Flyback converter circuit configuration Fig.2.6 Flyback converter with primary RC snubber Fig.2.7 General design of H-bridge inverter. Fig.2.8 Generic DC-link voltage waveform Fig.2.9 Bootstrap Driver Mosfet circuit. Fig.2.10 Output LCL filter of the inverter. 	
 Fig.2.4 CCM and DCM Flyback Current Waveforms Fig.2.5 Flyback converter circuit configuration Fig.2.6 Flyback converter with primary RC snubber. Fig.2.7 General design of H-bridge inverter. Fig.2.8 Generic DC-link voltage waveform. Fig.2.9 Bootstrap Driver Mosfet circuit Fig.2.10 Output LCL filter of the inverter. Fig.3.1 The controllers of PV inverter. 	
 Fig.2.4 CCM and DCM Flyback Current Waveforms Fig.2.5 Flyback converter circuit configuration Fig.2.6 Flyback converter with primary RC snubber Fig.2.7 General design of H-bridge inverter Fig.2.8 Generic DC-link voltage waveform Fig.2.9 Bootstrap Driver Mosfet circuit Fig.2.10 Output LCL filter of the inverter Fig.3.1 The controllers of PV inverter Fig.3.2 Design the controller of Flyback converter 	

Fig.3.4 Current, Voltage and Power characteristics of a PV module	52
Fig.3.5 Flowchart of the P&O MPPT algorithm.	53
Fig.3.6 Flowchart of the IC MPPT algorithm	54
Fig.3.7 Fixed and variable step size MPPT operation	57
Fig.3.8 Flowchart of the variable step size IC MPPT algorithm	60
Fig.3.9 Deferent control parts of the H-Bridge inverter	61
Fig.3.10 Inverter power stage diagram	62
Fig.3.11 Phasor diagram of ig and its two components	63
Fig.3.12 Voltage loop of the H-bridge inverter	64
Fig.3.13 Effect of the double-line frequency ripple on the current reference signal	64
Fig.3.14 Comparison of desired frequency and triangular waveform	66
Fig.3.15 Bipolar SPWM switching and Pulse width modulation	67
Fig.3.16 Unipolar Voltage switching Generation	68
Fig.3.17 Unipolar switching scheme	69
Fig.4.1 General view of grid connected PV inverter	72
Fig.4.2 Simulation Models of PV inverter	73
Fig.4.3 Model used for simulations.	73
Fig.4.4 MPPT Controller.	74
Fig.4.5 PV array output power with variable step size and fixed step size IC MPPT methods	75
Fig.4.6 PV array output power response time with variable and fixed step size IC algorithms	76
Fig.4.7 PV array output power due to sudden decrease in irradiation.	76
Fig.4.8 PV array output power due to sudden increase in irradiation.	77
Fig.4.9 Duty cycle for variable and fixed step size IC algorithms	77
Fig.4.10 PV array output power ripple for variable and fixed step size IC algorithms	78
Fig.4.11 PV array output power overshoot for variable and fixed step size IC algorithms	78
Fig.4.12 MATLAB model of autonomy PV inverter.	79

Fig.4.13 Duty-cycles generation.	80
Fig.4.14 Output control signals.	80
Fig.4.15 Inverter output voltage.	81
Fig.4.16 MATLAB Model of grid connected PV inverter.	82
Fig.4.17 Output voltages : output voltage of H-bridge inverter ,the output voltage with L filter , grid voltage, superposition h-bridge inverter and grid voltages .	CL 83
Fig.4.18 Final experimental PV inverter card.	84
Fig.4.19 Schematic of solar panel connections in the experiments PV system with the proposed MPPT controller.	85
Fig.4.20 PV array output performance (PV output current and the PV output voltage and output power) with fixed step size IC MPPT under constant irradiation (800W/m2)	PV 86
Fig.4.21 V array output performance(PV output current and the PV output voltage and F output power) with variable step size IC MPPT under constant irradiation (800W/m2)	PV 86
Fig.4.22 Schematic of grid connected solar inverter.	88
Fig.4.23 Control switches signals .	88
Fig. 4.24. Output voltage of the PV inverter	89
Fig. 4.25.Output voltage with LCL filter and FFT analyser	89
Fig. 4.26. Synchronisation grid tasting.	90

List of Tables

Table 2.1 Specification and requirements of PV inverter	31
Table 2.1 CCM and DCM characteristics of a Flyback Converter	.36
Table 2.3 The components of proposed prototype grid connected PV inverter	.55
Table 3.1 Principle of proposed variable step size ICMPPT method	.67
Table 3.1 Comparison of common variable step size Incremental Conductance MPPT with direcontrol	ect 68
Table 4.1 Electrical characteristics of Solarex MSX -60	.83

General introduction

The energy demand within residential and industrial sectors has been growing dramatically in recent years. The growth of human population and some improvements in standard f living will undoubtedly add pressure on energy supplies. Alternative highly reliable, energy solutions are becoming essential as the cost of fossil fuels rises. Renewable energy are considered as clean energy sources and the optimum use of these minimises the environmental impacts. These in fact naturally replenish themselves over a short time period by natural process such as sunlight, wind, rain, wave power, flowing water and geothermal heat, ocean energy, hydrogen and fuel cells [1-3].

Renewable energy is considered not only as a source of energy, but also as a promising solution to energy security,CO2 emissions and electricity costs etc. Therefore, these sources have become the subject of advanced research for extracting power with high reliability, lower cost and increased energy efficiency. Power generation from solar energy is one of the most promising renewable energies that attract the attention of researchers in recent years. Solar energy is in fact considered as a clean, renewable, in exhaustible, abundant in the most parts of the world at no cost and suitable for many applications. Solar energy can be utilized in two different ways. Solar is firstly used as a thermal source by capturing the heat as in space heating applications. Secondly, the incident solar irradiation is converted to electrical energy which is the most common utilization method [3,4]. Photovoltaic (PV)is currently the most popular renewable energy source compared to other renewable sources. PV is known asa simple, clean, noiseless, lowoperational and maintenancecost and environmentallybenign source. However, it has some drawbacks compared to conventional energy sources in particular its high fabrication cost, low energy conversion efficiency, and non-linear characteristics. The energy harvesting at maximum efficiency from PV sources remains a major problem [4].

PV power systems can be classified into three types: autonomous, grid connected and hybrid [4-6]. The autonomous systems are completely in dependent of other power sources. The common applications for this system are water pumps, power remote homes, cottages or lodges. However, autonomous systems in many cases require batteries for storage. The second category is the grid connected systems; that are used to reduce the consumption from the electricity grid and feed the surplus energy back in to the grid. The use of the smart grid technology has played an important role in managing the PV sources and the grid [7]. This system can produce significant quantities of high grade energy near the consumption point, avoiding transmission and distribution losses. In addition, DC/AC inverters are required by which many topologies and control strategies have been developed and improved continuously. The third category is the hybrid systems, in which a portion of their power is received from one or more additional sources. This system is selected for high energy demand.

To optimize the efficiency of large photovoltaic modules; a maximum power point tracker algorithm (MPPT) is introduced. A number of MPPT techniques has been studied in a variety of contexts. These techniques vary in complexity, accuracy, speed, oscillation around the MPP, hardware implementation sensor requirement [2,4]. The widely used MPPT techniques

are the perturbation and observation (P&O) algorithm, Incremental Conductance (IC) method and Hill Climbing (HC). For faster speed and more accuracy, MPPT controllers using particle swarm optimization (PSO) and genetic algorithms have been proposed. Moreover, fuzzy and neural-network methods are well adopted for handling nonlinearity in many applications. Despite these methods have a good performance in dealing with the nonlinear characteristics of the I–V curves; they require extensive computation the versatility of these methods is limited [8].

The perturbation and observation P&O, Incremental Conductance (IC) and Hill Climbing (HC) methods based on fixed iteration step size are simple and have good performances. However, they are characterized by slow convergence; oscillations in the PV power around the MPP and operation fail under rapidly changing atmospheric conditions. One way to reduce the oscilliations around the MPP is to use small perturbation step size but the speed of tracking MPPs remains slower. To acquire a fast response speed and to overcome the aforementioned drawbacks, a modified MPPT algorithms with variable step size have been the subject of many investigations, in which the step size is automatically adapted according to the derivative of power to voltage (dP/dV) of a PV panel. In general, the conventional IC MPPT algorithm uses a fixed step size to track the maximum power point (MPP) [9-11]. Thus, the tracking speed and accuracy are highly dependent on the fixed step size. The extracted power from the PV array using a large step size contributes to faster dynamics, but increases the losses in steady state due to large perturbations around the MPP. In contrast, applying small perturbation step size reduces the oscillationaroundMPP at the expense of slow tracking performance. . Thus, depending on each operational condition, the corresponding design should satisfactorily address the trade-off between the dynamics and steady state oscillations.In order to operate the PV system according to a suitable performance, a new MPPT methods based on variable step size has been developed [12].

A number of variable step-size, Incremental Conductance, MPPT algorithm with direct control has been proposed and investigated, in which the step size is automatically adjusted according to the first derivative of power with respect to voltage (dP/dV), to current (dP/dI) or (dP/dD). The variable step-size, Incremental Conductance MPPT algorithms are mostly similar to the conventional incremental conductance and the only difference is the step size calculation, a constant value N is often multiplied with the derivative (dP/dV, dP/dI,dP/dD).

To improve the efficiency of PV systems, DC/DC converters have been used in PV systems, Flyback converter is one of the most common topologies considered for PV modules because of its isolated property through a transformer. This also provides a simple topology with low cost, reduced number of semiconductor switches, operates over wide range of input voltage variation, and capable of achieving the optimal operation regardless of the load value.

In this thesis, a new variable step size Incremental Conductance MPPT algorithm with direct control has been proposed for the flyback converter DC/DCand also the unipolar PWM control for the H-bridge inverter. The overall system, flyback converter and the H-bridge inverter present the grid connected PV Inverter.

In the first chapter, we presented a general overview for the photovoltaic systems, an introduction for the smart grid, and finally the different topologies for the grid connected PV inverters. In the second chapter, the design process of the employed components for the developed grid connected PV inverter card is presented. In the third chapter, the design of the controller for different inverter sections is detailed, the proposed algorithm VSS IC MPPT (Variable Step Size IC MPPT) is described and the different PWM types for the control of H-bridge inverter is explained.

In chapter four, the proposed variable step size and fixed step size IC MPPT methods, the PWM control for the H-bridge inverter and also the connection with the electrical grid are tested and validated using Matlab/Simulink model and experimental prototype grid connected PV inverter is developed, using Flyback converter and the H-bridge inverter, which is controlled by a circuit based on Dspic30F4011. The different aspects of the system and parameters are implemented. Lastly, the conclusion of this thesis is made and proposed future research areas are given.

Chapter 1

The PV systems and the smart grids

Introduction	13
1-1 Introduction in the Photovoltaic systems	14
1-2 Photovoltaic characteristics.	15
1.2.1 Effect Temperature on Voc	15
1.2.2 Effect Irradiance on Ics	16
1.2.3 Maximum Tracking Point (MPPT)	17
1.3 Types of PV systems	17
1.3.1 Stand-Alone PV system	18
1.3.2 Grid-Tied PV system	18
1.3.3 Hybrid systems	19
1.4 Vision for future electricity systems	
1.4.1 Advanced Grid Features	22
1.4.2 Communication	23
1.4.3 Future-proof	24
1.5 PV inverters and Smart Grid	24
1.6 Topologies of Grid Connected PV systems	25
1.6.1 Centralized inverters	25
1.6.2 String Inverters	
1.6.3 Multi-String inverters	27
1-7 International Codes and Standards for Grid Connected PV system	
Conclusion	29

Introduction

Currently the number of decentralized source energy generation methods is increasing, ie photovoltaic wind and water based systems, this necessitates an increasing demand for smart power grid management schemes. In the Smart Grid of the future, the clients and customers of the source energy system are not just connected by conventional method via the electric grid but also via communication systems. The communicating clients are for example not only producers, but also consumers, storage systems, grid operators and trade customers. In this chapter photovoltaic energy management is studied in conjunction with the relationship between the smart grid technology and renewable source methods with different topologies of solar inverter configuration are presented.

1-1 Introduction in the Photovoltaic systems

Photovoltaic system is able to supply electric energy to a given load by directly converting sun energy through the photovoltaic effect. The PV modules are the main principal blocks; these can be arranged series or parallel to increase electric energy production. Typically supplementary equipment is necessary in order to transform energy into a useful form or store energy for future exploit. The resulting system will therefore be determined by the energy needs in a particular application. The basic PV cell model is presented in Figure 1.1 [1].



Figure 1.1 Equivalent circuit of PV cell model based on signal diode

Then the equations (1.1) through (1.3) could be obtained.

$$I_D = I_{SC} - I \tag{1.1}$$

$$I = I_S \left(e^{\frac{v}{n.Vt}} - 1 \right) \tag{1.2}$$

$$I = I_{SC} -_S \left(e^{\frac{v}{n.Vt}} - 1 \right) \tag{1.3}$$

Where

Isc : is the photo current;

Is : is diode reverse saturation current;

N : is diode ideality factor normally between 1 and 5;

 $VT = k^{T}/q$: is temperature voltage, which is 25.7 mV at 25°C;

K : is Boltzmann constant, which is 1.38 10-23 J/K;

T : is temperature in K and q is electron charge which is $1.6 \cdot 10^{-19}$ C.

1.2 Photovoltaic characteristics

Voltage and Current outputs of the PV modules is affected by temperature and irradiance [2]. Power electronics components of a photovoltaic system, such as grid-direct inverters have maximum and minimum voltage inputs. through rating of power electronics equipment, the variations of the temperate and the irradiance should be taken into account especially for the maximum power point tracking range of inverters.

1.2.1 Effect Temperature on Voc

A Photovoltaic module's voltage output is actually a variable value that is primarily affected by temperature. The relationship between module voltage and temperature is actually an inverse one. As elaborated in Fig.1.2 the module's temperature increases, the voltage value decreases and vice versa. It is important to put into consideration the cold and hot temperatures during PV design as shown in PV calculations in [3] [4] [5]. If the temperature of the module is less than the STC value of 25°C, the module's open circuited voltage, Voc value will actually be greater than the value listed on the module's listing label.



Fig.1.2: I-V characteristics of a PV module with temperature variation [3]

Photovoltaic module manufacturers will description the amount of change their modules testing in the form of temperature coefficients, most often in terms of a percentage per degree Celsius. For example for SM-55 solar modules at SIEMENS, the open circuited voltage temperature coefficient is $-0.077/{}^{0}C$.

This means that for every degree change in temperature, the module's open circuited voltage, Voc will change in the opposite direction by 7.7%. For example, if the PV module got colder by 1°C, the PV voltage would increase by 7.7%.

The rule in [4] [5] can be used to decide the averaged maximum and minimum voltages of the modules at these temperatures. Since the string voltage in this design will have a voltage, Voc is obtained to be 42 V. If we assume the working environment of the PV modules as recorded in [6], the functioning temperatures of the modules are assumed to be from -20° C to 40° C.

$$V_{OC} = V_{OC_STC} - [_{\gamma} * (T - T_{STC})]$$
(1.4)

Therefore using equation 1.4 for the worst ecological conditions we have the minimum and maximum Voc as 41.45 V and 42.18 V correspondingly. This gives the voltage change of approximately to $\Delta V = 0.73 V$.

1.2.2 Effect Irradiance on Ics

The quantity of current produced by a PV module is directly proportional to how bright the sun. Higher levels of irradiance will cause more electrons to flow off the Photovoltic (PV) cells to the load attached. However the amount of voltage produced by the PV module is affected by the irradiance value, but the effect is very small. As demonstrated in Fig. 1.3 the PV module's voltage changes very small with changing levels of irradiance. the SM-55 solar module has coefficient of current of $+0.0012 A/^{0}C$ [6].



Fig.1.3: I-V characteristics of a PV module with irradiance variation [3]

1.2.3 Maximum Tracking Point (MPPT)

Many MPPT methods have been reported, such as perturb and observe (P&O), incremental conductance(IC), neural network based (ANN) and fuzzy logic control as it has been said in [7], [8] [9]. Together with the efficiency, each method has its advantage and disadvantage for the tracking the maximum power. These approaches have been effectively used in standalone and grid-connected PV solar energy systems and operation well under sensibly slow and smoothly changing illumination conditions mainly caused by climate fluctuations, seen also in [2] [8]. In order to utilize the maximum power produced by the PV modules, The tools of power conversion has to be prepared with a maximum power point tracker (MPPT). This is a device which tracks the voltage at where the MPP is utilized at all times. It is generally implemented in the DC-DC converter, but in systems without a DC-DC converter the MPPT is included in the inverter control [7]. Maximum power point tracking will ensure that, PV modules operate in such away maximum voltage, Vmp and maximum current, Imp of the modules will be attained and produce maximum power, Pmax point, this illustrated on the Fig.1.4 are specified in the PV module data sheet of attached to it. The values are at standard test condition (STC) and they are called PV performance parameters.



1.3 Types of PV systems

Photovoltaic application can be very easy and simple, just a Photovoltaic module and load, for example as in the direct powering of a water pump motor, or more complex, as in a system to power a house. While a water pump may only need to operate when the sun shines, the house system will need to operate day and night. It also may have to run both AC and DC loads, have reserve power and may include a back-up generator. Depending on the system configuration, we can distinguish three main types of PV systems: stand-alone, grid-connected, and hybrid. In either case, basic PV system principles and elements remain the same. Systems are adapted to meet particular energy requirements by varying the type and amount of the basic elements. Ads as systems are modular; they can always be expanded, as power demands increases. In the PV systems we can be broadly classified in three major groups:

1.3.1 Stand-Alone PV system

In this type the PV system is isolated from the electric grid. The system described in Figure 1.5 is actually one of the most complex; and includes all the elements necessary to serve AC appliances in a common household or commercial application. An additional generator (e.g., diesel or wind) could be considered to improve the reliability but it is not necessary. The number of components in the system will depend on the type of load that is being served.

The DC/AC inverter could be eliminated or replaced by a DC/ DC converter if only DC loads are to be fed by the PV modules. It is also possible to directly couple a PV array to a DC load when alternative storage methods are used or when operating schedules are not of importance. Water pumping applications is a good example were a PV module is directly coupled to a DC water pump, water is stored in a tank through the day at any time energy is accessible.



Fig 1.5 Stand-Alone Photovoltaic System

1.3.2 Grid-Tied PV system

The grid connection PV systems are directly tied to the electric distribution network and do not need battery storage. The basic system configuration is disrupted in figure 1.6. Electric energy is either sold or bought from the local electric utility depending on the local energy load patterns and the solar resource variation during the day, this process mode requires an inverter to convert DC currents to AC currents. There are many benefits that could be obtained from using grid-tied PV systems instead of the traditional stand-alone schemes. These benefits are,[2],[1],[10]:

- fewer balance of system components are needed.
- Smaller PV arrays can supply the same load reliably.
- Comparable emission reduction potential taking advantage of existing infrastructure.

- Eliminates the need for energy storage and the costs associated to substituting and recycling batteries for individual clients. Storage can be included if desired to enhance reliability for the client.

- Giving many advantages of the existing electrical infrastructure.

- Efficient use of available energy. Contributes to the required electrical grid generation while the client's demand is below PV output.



Figure 1.6 Grid-Tied Photovoltaic System

1.3.3 Hybrid systems

These systems consist of combination of Photovoltaic modules and a complementary means of electricity generation such as a diesel, gas or wind generator. Schematically is a hybrid system shown in Figure 1.7. In order to optimize the operations of the two generators, hybrid systems typically require more sophisticated controls than stand-alone PV systems. For example, in the case of PV/diesel systems, the diesel engine must be started when battery reaches a given discharge level and stopped again when battery reaches an adequate state of charge. The back-up generator can be used to recharge batteries only or to supply the load as well. A common problem with hybrid PV/diesel generators is inadequate control of the diesel generator. If the batteries are maintained at too high a state-of-charge by the diesel generator, then energy, which could be produced by the PV generator is wasted. Conversely, if the batteries are inadequately charged, then their operational life will be reduced, this means the hybrid system is needed a high performance control for make a good management.



Figure 1.7. Schematic representation of a hybrid system.

1.4 Vision for future electricity systems

The development towards an overall smart grid vision can best be articulated by a vision of the electricity system of the future. In the latter period the electricity system is largely defined by large scale generation that produces power which flows in one direction to end users. The electricity system of the future will be defined by the services that electricity can provide, with bi-directional flow of power and information so that generation, distribution and end-users produce or use power while at the same time provide services that can support the operation of the grid (Figure 1.8). The integrated electricity system of the future can provide electricity in a more efficient manner, demonstrating net savings through better asset utilization of the grid, generation and end-use resources. Smart grid technologies will play a huge role in this, but technology on its own will not be sufficient, rather supportive policy and regulations the learning process needed to find technically and culturally relevant solutions in countries around the world can be accelerated [11].



Fig 1.8 Conception of Smart grid network

The aim of such a Smart Grid is a stable and optimized power supply in a changing system. The most important issues are:

- Increased power distribution efficiency and conservation

- Integration of Renewable: Smart Grids enable the integration of a massively increasing amount of decentralized electricity producers into the distribution grid.
- Lower Greenhouse Gas(GHG) and other gas emissions
- Dynamic Control: Smart Grids are better controllable. They allow mechanism to stabilize the grid and increase security of supply.
- Improve reliability of power quality and transmission
- Grid Synergies: Smart Grids enable more efficient use of energy through optimizing the local grid management and local energy balance at the customer.
- Cost Optimization: At long-term Smart Grids minimize the costs of the transition of the energy system and keep the electricity grid costs low.

Smart Grids need a lot of intelligent control and coordination between them. In this context, power production, especially photovoltaic due to its large share, plays a major role.

Grid-connected PV System comprises of PV panel, a DC/AC converter that capably connected to the grid. This system is used for power generation in places or sites accessed by the electric utility grid. If the PV system AC power is greater than the owner's needs, the inverter sends the surplus to the utility grid for use by others. The utility provides AC power to the owner at night and during times when the owner's requirements exceed the capability of the PV system [12]. Depending on the application and requirements PV system can either be a stand alone or hybrid system. The concept of smart grid is introduced in PV systems [13] depend on different ways of power utilization in the future. A smart grid construction with more strength and higher efficiency in power utilization is on schedule worldwide. Due to a large amount of new technologies and service will be raised, updated or replaced in smart grid from traditional power grid, a framework of the whole smart grid structure become necessary for the huge costly deployment, as well as the characteristics and functionalities. Smart Grid is a large and complicated concept which is still holding debate on its definition because of the expected emphasis addressed by each participant

PV inverters are ready to be fully integrated in a Smart Grid. At the moment, they are among the smartest devices in the grid. There are three main reasons for this statement :

- Advanced Grid Features
- Communication
- Future-proof

1.4.1 Advanced Grid Features

Inverters with their high speed and flexible internal control can apply a lot of functions for following a stable grid function. Such operations can prevent grid problems and therefor prevent outages and profit cuts. It is possible to install a lot more PV systems without grid enforcement than it would be without such characteristics.

With the term Advanced Grid Features we subsume several functions and behaviors. Some of them are already mandatory in some countries. Others are implemented but not activated. They can be turned on and configured if needed.

As an example the need for voltage control is given:

One of the biggest technical challenges for grid integration at the moment is the low voltage (LV) grid and its voltage boundaries. Voltage in LV is different at any location in the grid and in addition to that, it is different in each phase. PV inverters cannot cause harmful overvoltages because the internal interface protection has to disconnect the inverter at the moment the voltage reaches a defined limit (e.g. 110% of nominal voltage). But disconnection means a loss in production for existing PV plants or restrictions for further installations.

The inverters have many possibilities to influence the voltage even without losing energy.

Through supplying <u>reactive power</u>, an inverter can influence the voltage in the gird. The voltage can be raised by delivering reactive power and it can be lowered by consuming reactive power. A properly planned PV system can work with reactive power without causing energy losses.

There are several ways to control the reactive power. The possibilities range from the simplest way, a fixed displacement factor $\cos(\phi)$ to an optimized and fully configurable voltagedependent reactive power control functionality. In combination with communication, these local control functions can be dynamically configured during operation.

It is probable that even the most sophisticated reactive power control modes are not enough to keep the grid voltage within the required limits. Especially in low voltage networks, active power has the biggest influence on the voltage. therefore, influencing the active power supply of the PV inverter into the grid can prevent from overvoltage. The typical problem is overvoltage for only some moments at days with very high irradiation and low consumption at the same time. In these cases just a small reduction of produced power can prevent from overvoltage-caused complete disconnection. Because of a smart voltage-dependent power reduction the energy loss is much smaller than possible losses because of disconnection.

1.4.2 Communication

The system communication is very important for Smart Grids applications . PV inverters are most flexible with communication. There are two methods of communication:

- Information from the inverter can be sent to a control station or an automatic grid controller from the network operator. For example the actual power or the voltage at the inverter terminals can help to evaluate the actual situation of the grid and allow measurements if necessary.

- Communication to the inverter can be used to influence its actual operation.

When it is required e.g. because of temporary network restrictions, the output power of a PV system can be limited to any value. In the whole operating range, a reactive power setpoint can be sent via communication. So any active and reactive power value in the inverters operating range can be reached immediately.

But not only setpoits can be defined via communication. It is possible to configure control modes dynamically during operation and even without a restart of the inverter. This allows e.g. that a Smart Grid controller adjusts and optimizes the operation of all smart inverters in a specific area.

The objective of such a control is finding an operation optimum not only locally at one device but for a larger part of the electric system. This can prevent from losses in the grid on one side and at the same time prevent from a loss of power and earnings of the photovoltaic system.

The communication protocols used are flexible and it is possible to translate one protocol into another. At the moment, there is no standard communication protocol for Smart Grids. The next years will show if we will have a vast amount of different solutions, or if we can come to a small number of widely used protocols, which would lead to lower costs and simplification uses.

1.4.3 Future-proof

Smart Grids offer several advantages. Grid operators are able to integrate more PV systems into an efficient grid. Every customer who wants to have a PV system benefits from that. This is why we expect an increasing role of Smart Grid Functions required in the coming years. Standards and requirements already changed and are changing at the moment. Step by step, PV inverters have to do more.

A photovoltaic (PV) system delivers solar energy for 25 years and more. We expect that there will be several changes in grid integration rules in this period. Experience shows that it can be required that even retrofit of some features is possible.

Intelligent functions and communication will be mandatory for all size of PV systems in future. This is why it is important to pay attention to products that are ready for the future Smart Grid technology.

1.5 PV inverters and Smart Grid :

Smart grid technologies allow the electric grid to better adapt to the dynamic behaviour of renewable energy and distributed generation, this technology is an electricity network that uses digital and other complex technologies to observe and manage the transport of electricity from all generation sources to meet the varying electricity demands of end-users. Smart grids coordinate the needs and capabilities of all generators, grid operators, end-users and electricity market stakeholders to operate all parts of the system as efficiently as possible, minimising costs and environmental impacts while maximising system reliability, resilience and stability.

For the purposes of this roadmap, smart grids include electricity networks (transmission and distribution systems) and interfaces with generation, storage and end-users. while many regions have already begun to "smarten" their electricity system, all regions will require significant additional investment and planning to achieve a smarter grid. Smart grids are an evolving set of technologies that will be deployed at different rates in a variety of settings around the world, depending on local commercial attractiveness, compatibility with existing technologies, regulatory developments and investment frameworks. Figure 1.9 demonstrates the evolutionary character of smart grids.



1.6 Topologies of Grid Connected PV systems

There are different techniques and topologies available for grid connected PV systems which are categorized based on the number of power stages. In PV plants applications, various technological concepts are used for connecting the PV array to the utility grid. Each technology has its advantage and/or disadvantages compared to other, interns of efficiency and maximum power point tracking and the cost.

1.6.1 Centralized inverters

The topology illustrated in Figure 1.10 was based on centralized inverters that interfaced a large number of PV modules to the grid. The PV modules were divided into a string, each generating a sufficiently high voltage to avoid further amplification. These series connections were then connected in parallel, through string diodes, in order to reach high power levels [14]. For this architecture, the PV arrays are connected in parallel to one central inverter.



Fig.1.10: PV Central Inverters [15]

The organization is used for three-phase power plants, with power ranges between 10-1000 kW. The main advantage of central inverters is the high efficiency (low losses in the power conversion stage) and low cost due to usage of only one inverter. The drawbacks of this topology are the long DC cables required to connect the PV modules to the inverter and the

losses caused by string diodes, mismatches between PV modules, and centralized maximum power point tracking [15] [7].

1.6.2 String Inverters

The present technology consists of the string inverters and the ac module. The string inverter, shown in Figure 1.11 is a reduced version of the centralized inverter, where a single string of PV modules is connected to the inverter. The input voltage may be high enough to avoid voltage amplification [14]. This configuration emerged on the PV market in 1995 with the purpose of improving the drawbacks of central inverters. Compared to central inverters, in this topology the PV strings are connected to separate inverters. If the voltage level before the inverter is too low, a DC-DC converter can be used to boost it. For this topology, each string has its own inverter and therefore the need for string diodes is eliminated leading to total loss reduction of the system. The configuration allows individual MPPT for each string; hence the reliability of the system is improved due to the fact that the system is no longer dependent on only one inverter compared to the central inverter topology [15]. The mismatch losses are also reduced, but not eliminated.

This construction increases the overall efficiency when compared to the centralized converter, and it will reduce the price, due to possibility for mass production [14] [7]. The photovoltaic modules in the given topology are linked in a structure whereby they end up forming a string; the voltage from the PV array ranges between 150-450 V [9].



Fig.1.11: String Inverters . [15]

1.6.3 Multi-String inverters

As this current and future topology, multi-string inverter configuration became available on the PV market in 2002 being a mixture of the string and module inverters [15]. The multistring inverter depicted in Figure 1.12 is the further development of the string inverter, where several strings are interfaced with their own dc–dc converter to a common dc–ac inverter. This is beneficial, compared with the centralized system, since every string can be controlled individually [14] [7]. The power ranges of this configuration are maximum 5 kW and the strings use an individual DC-DC converter before the connection to a common inverter. The topology allows the connection of inverters with different power ratings and PV modules with different currentvoltage (I-V) characteristics. MPPT is implemented for each string, thus improved power efficiency can be obtained [15]. This gives a flexible design with high efficiency, and will probably become standard where centralized and string converters are used today [7].



Fig.1.12 Multi-String Inverters.[15]

1.6.4 Module Inverters

Module Inverters topology shown in Figure .1.13 is the present and future technology consists of single solar panels connected to the grid through an inverter. A better efficiency is obtained compared to string inverters as MPPT is implemented for every each panel [15]. By incorporating the PV module and the converter into one device, the possibilities of creating a module based "plug and play" device arises, and it can then be used by persons without any knowledge of electrical installations. In this configuration the mismatch losses between the PV modules is removed and it is possible to optimize the converter to the PV module, and

thus also allowing individual MPPT of each module. Since there will be need for more devices then with the previous mentioned configurations, it will give the benefit of large scale production, and thus lower prices. On the other hand the input voltage will become low, requiring high voltage amplification, which may reduce the overall efficiency [14].



Fig.1.13: Module inverters [15]

1.7 International Codes and Standards for Grid Connected PV system

In the grid connected photovoltaic systems there are many standards on the market dealing with the interconnection of distributed resources with the grid [7]. In this context PV system is of importance where all practice for wiring, design and installation has been explained. This thesis is limited to International Electro technical Commission (IEC), Institute of Electrical and Electronics Engineers (IEEE) and National Electrical Code (NEC). Standards and codes governing the design of the proposed PV system at NTNU electro building is based on PV electrical installations practices and interfacing with grid. In the standard [3]

IEEE 929-2000: Recommended Practice for Utility Interface of Photovoltaic (PV) Systems which gives the guidance to PV system practices. These practices include power quality and protection functions [16].

The IEEE 929 standard also containing UL 1741 standard which has been used as the key to select inverters used in this design.

The IEC standard has been discussed in [7] and they show to give out the characteristics of PV system and grid interface at the point of common coupling (PCC).

National Electrical Code in article 690 Photovoltaic power systems [17] as well as explain in literatures [18] and [10] shows the necessity and important information for proper installation of PV system.

The 690 code explain most of the important information in both design aspects and installation. Some of this important information includes;

- PV system conductors and coding.
- Grounding system and Module connection
- PV source circuits, PV Inverter output circuits and circuit routing.

• Identification of equipment used and system circuit requirements i.e. Open Circuit voltage and short-circuit current.

Conclusion

In this chapter an overview of photovoltaic generation systems and smart grid methodology has been discussed. The characteristics and the behaviour of these system with differing climatic changes encountered by the PV system have been explained as well as differing topologies and structures for the grid connected PV inverter are described. Following this the importance of the smart grid and the relationship of this to renewable energy sources have been discussed in detail. Subsequently, an explanation of the conditions and international standards for the grid connected PV inverters was presented. The thesis then goes on to discuss the different components of grid connected PV inverter which were then studied alongside design methodologies in the next chapter.

Chapter 2

Design of the PV-Inverter

Introduction	31
2.1 Design of Input LC Filter	32
2.1.1 Input Inductance (L_{PV})	32
2.1.2 Input capacitance (C_{PV})	
2.2 Design of Flyback Converter	33
2.2.1 Original of the flyback converter	
2.2.2 Flyback Modes of Operation: DCM vs CCM	35
2.2.3 Designing the power stage of flyback converter	
2.3 Design of H-bridge inverter	45
2.3.1 Theory of operation	46
2.3.2 Calculation of DC-link Capacitor	46
2.3.2.1 Electrolytic Capacitors vs Film Capacitors	47
2.3.1.2 Sizing the DC-link Capacitor	48
2.3.3 Switching Circuit Configuration	
2.3.4 Driver and isolation Switching Circuit	49
2.3.4 .1 Determining bootstrap capacitance, CB-STRAP	50
2.3.4 .2 Determining bootstrap diode, DBS, and resistor, RC	52
2.4 Design of output Filter	53
2.5 Components for the implementation	55
Conclusion	56

Introduction:

In previous chapter different topologies of grid connected inverters were discussed, building on this chapter two goes on to examine the design of the component parts of the grid connected PV inverterin detail. Specific aspects of the design of a power-electronic inverter are examined and many issues such as the selection of silicon devices, magnetics, capacitors, gate drives, grid performance, current and voltage protection, control strategies and implementation etc. are discussed. The selected inverter design was presented in chapter 1, and is illustrated in Figure 2.1. An overview of the designed components for the flyback converter and the H-Bridge inverter and the output will now be presented in the following chapter.



Fig 2.1 Basic diagram of PV inverter

The design of the inverter is based on the specifications given in this thesis, the selected specification and requirements shows in the table 2.1 below:

Parameters	Values	
Vpvmax	42 V	Maximum Input PV voltage
Vpvmin	32 V	Minimum Input PV voltage
Isc	27 A	Short circuit Input PV currant (Imax)
Vout	325 V	Output voltage (nominal)
Pout	960 W	Output power
fsw	50 kHz	Switching frequency of flyback Converter
fsw(AC)	20kHz	Switching frequency of H-Bridge Inverter
Vout ripple	1% , 3,2 V	Maximum ripple voltage

Table 2.1. Specification and requirements of PV inverter

In this chapter we will design the deferent sections of the grid connected PV inverter, there are four mains sections:

- Design of Input LC Filter
- Design of Flyback Converter
- Design of H-bridge inverter
- Design of output Filter

These parts calculated and explained with accurate equations in the next titles.

2-1 Design of Input LC Filter

The input parameters (input filter) as applied to the input voltage from the photovoltaic system are very important. These parameters are DC inductor L_{pv} and input capacitor C_{pv} . There are direct formulae that have been used by various literatures to estimate these parameters as summarized in [7] [19] [20] [21].

2.1.1 Input Inductance (L_{PV})

In generally designs, the inductor is always given in a certain range provided in the data sheet. However it is wise to estimate the converter inductor directly if no data sheet available. The estimation is calculated using equation 2.1 [21].

$$L_{PV} = \frac{V_{IN} \cdot (V_{out} - V_{IN})}{\Delta I_L \cdot V_{out} \cdot f_s}$$
(2.1)

Were:

 L_{PV} : PV input inductor.

 ΔI_L : Estimated inductor ripple current.

V_{out} : Desired output voltage.

 V_{IN} : Typical input voltage.

 f_s : Switching frequency.

The inductor ripple current can be estimated by 20% to 40% of the output maximum current. This can be found by using equation 2.2 [21].

$$\Delta I_L = 0.2 \cdot I_{OUT_max} \cdot \frac{V_{OUT}}{V_{IN}}$$
(2.2)

2.1.2 Input capacitance (C_{PV})

After calculating the output PV inductor, then the input capacitance C_{PV} can be obtained easily by using the analysis done in [21]. The analysis also assumes the continuous conduction mode (CCM) of the flyback converter DC/DC.

The irradiance and temperature are not constant, this variations are discussed in section 1.3 of this thesis, the capacitance will see the voltage ripple from the PV array MPP as , ΔV_{PV} . As temperature changes from -20°C to 40 °C the open circuit voltages also sees these changes and the open circuit of the PV string voltage change is by, $\Delta V_{PV} = 0.73$ V (Calculated in Chapter 1).

So, by using equation 2.3 [19] the PV input capacitance C_{PV} that is important to voltage source inverters (VSI). This converts the model of the PV modules and seen as voltage source by the inverter. It is also keeps the voltage constant and reduces power oscillation at the input.

$$\Delta P_{PV} = \frac{D \cdot V_{PV}}{4 \cdot f_{SW}^2 \cdot L_{PV} \cdot C_{PV}}$$
(2.3)

Therefore, the input capacitance is then estimated as [19]:

$$C_{PV} = \frac{D \cdot V_{PV}}{4 \cdot f_{SW}^2 \cdot L_{PV} \cdot \Delta P_{PV}}$$
(2.4)

2.2 Design of Flyback Converter

The flyback converter is used in DC/DC conversion with galvanic isolation between the input and the outputs. The flyback converter is a buck-boost converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with an additional advantage of isolation. The flyback stricture is chosen in this thesis for add in the global system (grid connected PV inverter), many points will study for this structure :

- Original of the flyback converter
- Flyback Modes of Operation DCM vs CCM
- Designing the power stage of flyback converter

2.2.1 Original of the flyback converter

Flyback converter is based on the buck-boost converter. Its derivation is illustrated in Figure 2.2. In the flyback converter divided into four phases, the firstly is shown in Figure 2.2(a) depicts the basic buck-boost converter, with the switch realized using a MOSFET or IGBT and one diode .The second phase shown in Figure. 2.2(b), the inductor winding is constructed using two wires, with a 1:1 turn's ratio. The basic role of the inductor is unchanged, and the parallel windings are equivalent to a single winding constructed of larger wire. In Fig. 2.2(c) shown the third phase, the connections between the two windings are broken and isolated. The first winding is used while the transistor Q1 conducts, while the other winding is used when diode D1 conducts. The total current in the two windings is unchanged from the circuit of Figure 2.2(b); however, the current is now distributed between the windings differently. The magnetic fields inside the inductor in both cases are identical. Although the two-winding magnetic device is represented using the same symbol as the transformer, a more descriptive name is "two winding inductor". This device is sometimes also called a "flyback transformer". Unlike the ideal transformer, current does not flow simultaneously in both windings of the flyback transformer. The lastly phase shown in Figure 2.1(d) illustrates the usual construction of the flyback converter. The MOSFET source is connected to the primaryside ground, this is very important advantage for simplifying the gate drive circuit. The transformer polarity marks are reversed, this is to get a positive output voltage. The turn's ratio between the primary and secondary self in the flyback transformer is introduced; this allows better converter optimization, this optimisation of duty cycle switch control.


Figure 2.2: Derivation of the flyback converter

2.2.2 Flyback Modes of Operation: DCM vs CCM

Flyback converter schematic is shown in figure 2.3. Its main parts are the transformer, the primary switching MOSFET Q1, secondary rectifier D1, input and output capacitor C1,C2 and the PWM controller IC. Depending on the design of T1, the Flyback converter can operate in two deferent modes; the first mode is Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). Each mode has advantages and disadvantages. [22]



Figure 2.3: Flyback Schematic [23]

In the first mode Discontinuous Conduction Mode (DCM), all the energy stored in the transformer core is delivered to the secondary during the turn off phase, and the primary

current stored in the first indictor falls back to zero before the Q1 switch turns on again. For the second mode Continuous Conduction Mode (CCM), the energy stored in the primary transformer is not completely transferred to the secondary; that is, the Flyback transformer current (ILP and ISEC) does not arrive at zero before the next switching cycle. The difference between Continuous Conduction and Discontinuous Conduction Mode in terms of Flyback primary and secondary current waveforms is shown in figure 2.4 blow.



Figure 2.4: CCM and DCM Flyback Current Waveforms [22]

Table 2.2 shows the characteristics of the flyback converter for two modes, in CCM and DCM operation.

	DCM	CCM
Input Impedance	$Zin = \frac{2f_sL}{D^2}$	$Zin = \frac{D'^2 R}{D^2}$
Voltage Transfer Characteristics (Vout/Vin)	$M = \frac{Vout}{Vin} = D\sqrt{\frac{R}{X}}$	$M = \frac{Vout}{Vin} = \frac{D}{D'}$
Mode of Operation Criterion	$D^{*2} R > X$	$D^{\prime 2} R < X$

1 a 0 0 2.2. CONTAIN DONTONICIONSUES OF a LIVUACK CONVENCE. [24]
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In Discontinuous Conduction Mode (DCM) operation requires a higher peak currents (Ipeak) to deliver the required output power compared to Continuous Conduction Mode (CCM) operation. This translates to a higher RMS current rating on the primary switch Q1 and output

capacitor C2, and bigger conduction losses in the transformer windings. When these higher peak and RMS current limits the realization of design requirements, (e.g. larger output capacitor C2 required or very high conduction loss on the MOSFET and transformer), switching of the mosfet in CCM mode is advised. The advantages of each mode are listed below: [22]

In CCM mode:

- ► Lower primary and Secondary RMS current factor.
- > Smaller output capacitor this means lower ripple current.
- Peak switch and diode current.
- Cross regulation for multiple outputs.
- > Flux ripple excursion in transformer core.
- > RMS loss in transformer windings.

In DCM mode:

- ➢ Faster transient response.
- Smaller transformer.
- > Ease of feedback loop and current loop compensation.
- > Zero reverse recovery loss on rectifier diode.
- ➢ Low turn-on loss for the switch.

2.2.3 Designing the power stage of flyback converter [25-29]

In the Flyback Topology There are many standard power converter topologies available to choose from, each structure has advantages and disadvantages [24]. After careful consideration, taking into account factors such as low power, simplicity, isolation, input and output ripple currents, and low cost, the flyback configuration was chosen, after studding the deference between DCM and CCM mode, also chosen the design in Continuous Conduction Mode (CCM), The basic flyback converter topology is shown in Figure 2.5.



Figure 2.5. Flyback converter circuit configuration.

For design the Flyback converter there are six important points studied, in this part the deferent components are designed step by step:

STEP 01: Maximum Duty Cycle and Turns Ration

In this decision to be made is what the maximum duty cycle , should be. The duty cycle is the ratio of on-time of Q1, Figure 2.5, to full period, or D = ton/T. In a Continuous Conduction Mode flyback converter the maximum duty cycle Dmax will determine the turn's ratio of the transformer and effect the maximum voltage Vpeak stress on the switching part. For this design and requirements of the MPPT control, a maximum duty cycle Dmax of 65% was selected. Limiting the duty cycle increases the number of controller ICs to choose from because many available today have maximum duty cycle limitations of 65%.

The DC transfer function of a CCM flyback converter is: [30] [31]

$$\frac{V_{O} + V_{D}}{V_{IN(MIN)} - V_{Rds(ON)}} = \frac{1}{N} \left(\frac{D_{MAX}}{1 - D_{MAX}} \right)$$
(2.5)

where:

V₀: equals the output voltage, 325 V,

 V_D = forward voltage drop across rectifier D1, assumed to be 0.8V,

$$V_{IN} = 32$$
 to 42V, $V_{IN}(min) = 32V$,

 $V_{Rds(on)}$ = on voltage drop across MOSFET Q1,equal to $R_{ds(on)} \cdot I_{RMS}$ (primary), assumed to be 1V,

N = turns ratio, equal to Np/Ns,

Ns = number of transformer secondary turns,

Np = number of transformer primary turns,

D = duty cycle.

The maximum duty cycle, D_{max} =0.65, occurs at minimum input voltage Vin. The turns ratio is inversely proportional to the peak primary current, IPEAK, and directly proportional to the voltage stress on the switching part. So the IPEAK will not become unreasonably high and the voltage stress on the MOSFET will be kept as low as possible, the turns ratio is rounded up only to the next integer value, 9, or simply nine secondary turns for every one primary turn. Recalculating equation (2.5) results in an actual Dmax of 65%.[25] [26] [27]

STEP 02: Switching Frequency

For choose the optimum frequency work, the decision is not quite that clear cut. Gate charge currents, core losses, and switching losses increase with higher switching frequencies; peak currents and, consequently, I^2R Jol losses increase with lower switching frequencies. [29] A compromise must be reached between component size, current levels, and acceptable losses. Synchronization with other systems and backward compatibility may also be deciding factors. For this design, a fixed frequency (fsw) of 50kHz was chosen. At Dmax equal to 65%, ton(max) becomes 13µs. [27]

STEP 03: Transformer Design

The most important thing in a flyback converter is the transformer; it is actually a coupled inductor with multiple windings. Transformers provide coupling and isolation whereas inductors provide energy storage. The energy stored in the air gap of the inductor is equal to [32] [31]:

$$E = \frac{L_P (I_{PEAK})^2}{2}$$
(2.6)

where:

E: is in Joules.

L_P: is the primary inductance in Henry's.

I_{PEAK}: is the peak primary current in Amperes.

When the switch is on, D1 (from Figure 2.5) is reverse biased due to the dot configuration of the transformer. No current flows in the secondary windings and the current in the primary winding ramps up at a rate of: [31] [29]

$$\frac{\Delta I_L}{\Delta t} = \frac{V_{IN(MIN)} - V_{Rds(on)}}{L_P}$$
(2.7)

Where $V_{IN(min)}$ and $V_{Rds(on)}$ were defined previously and Δt is equal to $t_{on(max)}$ at $V_{IN(min)}$. Output capacitor, C_{OUT} , supplies all of the load current at this time. Because the converter is operating in the CCM mode, ΔI_L is the change in the inductor current which appears as a positive slope ramp on a step. The step is present because there is still current left in the secondary windings when the primary turns on. When the switch turns off, current flows through the secondary winding and D1 as a negative ramp on a step, replenishing C_{OUT} and supplying current directly to the load. Based on (2.7), the primary inductance can be calculated given an acceptable current ripple, ΔI_L . The calculate of primary inductance should then be design within the limit of maximum duty cycle : [22]

$$L_{p_{max}} = \frac{V_{DCmin} \cdot D_{max}}{I_P \cdot f_{SW}}$$
(2.8)

For the demo board design, ΔI_L was set to equal one-half the peak primary current. For a CCM flyback design, the peak primary current is calculated based upon (2.9). [30] [25]

$$I_{PEAK} = \left(\frac{I_{OUT \ (MAX \)}}{N}\right) \cdot \left(\frac{1}{1 - D_{MAX}}\right) + \frac{\Delta I_L}{2}$$
(2.9)

By replacing ΔI_L with $\frac{1}{2}(I_{PEAK})$, $I_{OUT(max)}$ with 27A, Dmax with 0.65, and N with 9 as detailed earlier, the peak primary current is calculated to be 103,87 A. The root mean square, RMS, current of a ramp on a step waveform is defined in (2.10). [30] [25]

$$I_{RMS} = \sqrt{\frac{t_{on\,(max\,)}}{T}} \left((I_{PEAK})^2 - \Delta I_L \cdot I_{PEAK} + \frac{(\Delta I_L)^2}{3} \right)$$
(2.10)

The core material was chosen to be manganese zinc ferrite EE55. Because the inductor is driven in one quadrant of the B-H plane only, a larger core is required in a flyback design. Because this converter is operating in the CCM at a relatively low frequency, the maximum peak flux density, B_{max} , is limited by the saturation flux density, B_{sat} . Taking all this into consideration, the minimum core size is determined by (2.11). [30]

$$AP = \left(\frac{L_P \cdot I_{PEAK} \cdot I_{RMS} \cdot 10^4}{420 \cdot k \cdot B_{MAX}}\right)^{1.31}$$
(2.11)

Where

AP = the core area product in cm⁴,

k = winding factor, equal to 0.2 for a continuous mode flyback,

 $B_{max} \gg B_{sat}$, or 0.33 Telsa at 100°C.

The result of (2.11) is compared to the product of the winding area, Aw (cm²), and effective core area, Ae (cm²), listed in the core manufacturer's data sheet. For this design, a EE55 core met the minimum criteria. The minimum number of primary turns is determined by: [30]

$$N_P = \frac{L_P \cdot I_{PEAK} \cdot 10^4}{B_{MAX} \cdot Ae}$$
(2.12)

If adding an air gap, the hysteresis curve of the magnetic material is really tilted, requiring a lot higher field force to saturate the core. The air gap is calculated using (2.13). [30] [25]

$$gap = \frac{\mu_o \cdot \mu_r \cdot (N_P)^2 \ Ae \cdot 10^{-2}}{L_P}$$
(2.13)

STEP 04 : MOSFET Selection

The part of switching in a flyback converter must have a voltage rating high enough to handle the maximum input voltage and the reflected secondary voltage [30] [25] [26], not to mention any leakage inductance induced spike that is inevitably present. Approximate the required voltage rating of the MOSFET using (2.14).

$$V_{ds} = \left[\left(V_{IN(max)} + V_L \right) + \left(\frac{N_P}{N_S} \right) \cdot \left(V_O + V_D \right) \right] \cdot 1.13$$
(2.14)

Where V_{ds} = the required drain to source voltage rating of the MOSFET, V_L = the voltage spike due to the leakage inductance of the transformer, estimated to be thirty percent of $V_{IN(max)}$, and the additional 1.3 factor includes an overall thirty percent margin.

In the flyback converter presented, the required minimum voltage rating of the MOSFET calculates to be 325V. An IRFP460 N-channel power MOSFET was chosen [28]. This device has a voltage rating of 500V, a continuous DC current rating of 20A, and an Rds(on) of only 0.4W. By consulting the typical gate charge Vgs. gate-to-source voltage waveform in the manufacturer's data book, calculating the average current required to drive the gate capacitor of the FET is possible:

$$I_{gate} = Q_{max} \cdot f_{SW} \tag{2.15}$$

 Q_{max} is the total gate charge in Coulombs, estimated to be 70nC based upon a gate to source voltage of 15V and a drain to source voltage of 500V. According to (2.15), the average supply current of the controller, I_{VDD} , needs to increase by 4.9mA to switch the gate at the selected operating frequency. This FET will experience both switching and conduction losses. The conduction losses will be equal to the I²R losses, as shown by (2.16).

$$P_{cond} = (I_{RMS})^2 \cdot R_{ds(on)}$$
(2.16)

STEP 05: Diode Selection

The best choose for this application is the Schottky rectifiers, it's have a lower forward voltage drop than typical PN devices, making it the rectifier of choice when considering reducing converter losses and improving overall efficiency. Selecting the appropriate Schottky for a specific application depends mainly on the working peak reverse voltage rating, the peak repetitive forward current, and the average forward current rating of the device [30]. If the maximum working peak reverse voltage is exceeded the reverse leakage current will rise above its specified limit. The peak reverse voltage that the device will be subjected to is equal to the reflected maximum input voltage minus the voltage drop across the FET added to the output voltage. The maximum average forward current rating of the device must not be exceeded if the junction temperature of the device is to remain within its safe operating range. Because all current to the output capacitor and load must flow through the diode, the average forward diode current is equal to the steady-state load current. The peak

repetitive forward current is equal to the reflected primary peak current [29]. An MUR1640 Schottky rectifier from Motorola met the requirements for the demo board design. This device is a common cathode dual Schottky with a forward voltage drop of 0.47V and a working peak reverse voltage rating of 600V. The average rectified forward current rating is specified at 8A per leg, 16A total, and the peak repetitive forward current is rated for 16A per leg, or a total of 32A. Power loss in the Schotty is the summation of conduction losses and the reverse leakage losses. Conduction losses are calculated using the forward voltage drop and the average forward current. The MUR1640 will have conduction losses equal to 4.7W. Reverse leakage losses, which are dependent upon the reverse leakage current, the blocking voltage, and the on-time of the FET, are calculated to be 0.05W. Heat sink selection is once again based upon the required thermal resistance of the heat sink to air interface in order to maintain a junction temperture of less than 125°C. [30]

STEP 06 : Input and Output Capacitors

In this part, the input capacitors are chosen based upon their ripple current rating and their rated voltage. The RMS value of the ripple current is calculated by adding the RMS current of the ramp on a step shaded waveform during t_{ON} with the RMS value of the average input current during t_{OFF} . Because this example uses a duty cycle that is very close to 50%, this RMS current is almost equal to the primary RMS current calculated in (2.10). The actual capacitor value is not that critical as long as the minimum capacitance gives an acceptable ripple voltage determined by the following equation: [30]

$$C_{min} = \frac{I_{RMS}}{8 \cdot f_{SW} \cdot \Delta V} \tag{2.17}$$

The output capacitors are also chosen based on their low equivalent series resistance (ESR), ripple current and voltage ratings, and (2.17). The ripple current that the output capacitor experiences is a result of supplying the load current during the FET conduction time and its charging current during the FET off-time.

STEP 07: Calculation of the wire diameter for each winding

The Diameter of wire is determined based on the RMS current through the wire. The current density is typically 5A/mm2 when the wire is long (>1m). When the wire is short with a small number of turns, a current density of 6-10 A/mm2 is also acceptable. [33] Avoid using wire

with a diameter larger than 1 mm to avoid severe eddy current losses as well as to make winding easier. For high current output, it is better to use parallel windings with multiple strands of thinner wire to minimize skin effect [34].

In order to determine the required wire size the RMS current for each winding should be determined. [22]

Primary winding RMS current:

$$I_{P_{RMS}} = I_P \cdot \sqrt{\frac{D_{max}}{3}} \tag{2.18}$$

Secondary Winding RMS current:

$$I_{sec_{RMS}} = I_{sec_{pk}} \cdot \sqrt{\frac{1 - D_{max}}{3}}$$
(2.19)

STEP 08: Primary RC Snubber

In Figure 2.6, an RC snubber circuit, used to damp the ringing on the drain of the FET. The resistor provides damping for the LC resonance of the power circuit, and the series capacitor prevents the voltages at the power stage switching frequency from being applied across the resistor. The capacitor is sized to allow the resistor to be effective at the ringing frequency. The RC snubber is best placed directly across the semiconductor that is to be protected. [35]

If using a current sense resistor in series with the FET, make sure that the snubber is connected to the top of the sense resistor, not to ground. When you do this, the sense resistor will not see the current spike at turn-on when the snubber capacitor is discharged.



Figure 2.6: Flyback converter with primary RC snubber.

In order to damp the ringing properly, we need to calculate the characteristic impedance of the resonant circuit. This is given by: [35]

$$Z = R_{sn} = 2\pi f_r L \tag{2.20}$$

The ringing will be well damped if we use a snubber resistor equal to the characteristic impedance of the ringing. We therefore use the design point of R=Z to select the resistor. The snubber capacitor is used to minimize dissipation at the switching frequency, while allowing the resistor to be effective at the ringing frequency. The best design point to start with is the impedance of the capacitor at the ringing frequency equal to the resistor value: [35]

$$C_{sn} = \frac{1}{2\pi f_r R} \tag{2.21}$$

In order to complete the design of the PV inverter, the next section will be design the Hbridge inverter.

2.3 Design of H-bridge inverter

The essential parameters for the H-bridge inverter design are listed in Table 2.1. Since the design primarily focuses on the control and the grid synchronization method of the inverter, the efficiency target of the inverter is not specified because it is outside of the scope. Although maximizing efficiency is not the focus of this work, loss considerations still drive selection of a viable converter topology. The figure 2.7 illustrates a general design for H-bridge inverter:



Fig 2.7 General design of H-bridge inverter.

Many parameters will designed in this section, the mains study included in these points:

- Theory of operation
- Calculation of DC-link capacitor
- Switching circuit configuration
- Driver and isolation switching circuit

These points explained in the titles below.

2.3.1 Theory of operation

A H-bridge topology is used to implement the DC/AC inverter. Through positive output half cycle, Q1 is sine pulse width modulated while Q4 is closed. During negative output half cycle, Q2 is sine pulse width modulated while Q3 is closed. The switching frequency of the high side and low side MOSFET's are 20 kHz. This switching technique produces 50 Hz AC sine wave across the output capacitor C_f after inductor L_i .

Q1 to Q4 are chosen to be ultrafast Mosfet's, IRFP460 which offers balanced conduction and switching losses at 20 kHz. Low conduction loss Mosfet's is essential for all switches since conduction loss is the dominant factor while switching loss is not at 50 Hz.

Each arm (or leg) of the full Bridge is driven using a high voltage gate driver IC, TLP250, with bootstrap power supply technique for the high side. Using TLP250 eliminates the requirement for an isolated power supply for the high side drive. This translates into augment efficiency and parts count reduction of the general system.

The benefits of the full bridge stricture and switching technique are:

- 1. Very high efficiency since Q1 and Q2 co pack diodes are not subjected to the freewheeling current and Q3 and Q4 have majority of conduction loss and very little switching loss.
- 2. Operate from single DC bus supply eliminating the need for a negative DC bus.
- 3. No cross conduction possibility since switching is done on diagonal device pair only at any time (Q1 and Q4 or Q2 and Q3).
- 4. Mosfet's are driven using high voltage gate driver TLP250 with bootstrap technique.

2.3.2 Calculation of DC-link Capacitor

This part discusses the two types of capacitors that can be used as the DC-link buffering capacitor. A short comparison is made based on their life time and power decoupling ability. Methods of ensuring the inverter's power quality while using a capacitor that has a small capacitance are also discussed. Finally, the calculation of the DC-link capacitance is shown in this part.

For this two points discussed for this calculation:

- Electrolytic Capacitors vs Film Capacitors
- Sizing the DC-link Capacitor

These points explained in the next titles.

2.3.2.1 Electrolytic Capacitors vs Film Capacitors

The input capacitor is very important for the power decoupling between the input power to the inverter and their output power to the utility grid [42] [43]. In general, electrolytic capacitors are used for their large capacitance and low cost. However, in the photovoltaic applications where the inverters are usually exposed to outdoor temperatures, the lifetime of such electrolytic capacitors is shorten drastically according to the equation below [36] [37]:

$$L_{op} = L_{op}(0). 2^{\frac{T_0 - T_h}{\Delta T}}$$
(2.22)

Where:

 L_{op} : is the operational lifetime.

 $L_{op}(0)$: is the specified operational lifetime at the hot spot temperature .

 T_0 : can be found in the product datasheets.

 T_h : is the operating temperature .

 ΔT : is the degree Celsius increase that would results in half the operational life (also can be found in the product datasheet).

characteristically, $L_{op}(0)$ is between 3000 to 6000 hours (8 months to 16 months) at 85°C for electrolytic capacitors with rated voltage above 400V [38].

In the photovoltaic applications, since most PV module manufactures over 25 year warranties on 80% of the initial efficiency and five years warranty on materials and workmanship [36],the lifetime of the electrolytic capacitors have become a major limiting component inside a photovoltaic DC/AC inverter.

On another side the film capacitors are a clear the alternative given their long life expectancy and wide operating temperature range. Unfortunately, the film capacitors are more expensive than the electrolytic ones in term of cost per farad, hence the size of the capacitance has to be smaller to keep the price of the capacitor acceptable. However, smaller capacitance would weaken the power decoupling ability of the DC-link capacitor which may cause DC-link voltage fluctuations that lead to distortion of the inverter output current to the grid.

2.3.2.2 Sizing the DC-link Capacitor

To limit the magnitude of the double-line frequency ripple voltage to the specified level, the DC link capacitor is sized according to the following equations: Assuming the grid voltage and the grid current are [39] [42] [43]:

$$v_g(t) = V_g \cos(\omega_g t) \tag{2.23}$$

$$i_g(t) = I_g \cos(\omega_g t - \partial)$$
(2.24)

Then the instantaneous output power can be easily obtained as:

$$P_{out}(t) = S\cos\partial + S\cos(2\omega_g t - \partial)$$
(2.25)

where S is the apparent power which has a unit of VA. The nominal voltage V^n_{dc} of DC-link is:

$$V_{dc}^{n}i_{dc}(t) \cong S\cos[\theta + S\cos[2\omega_{g}t - \partial]$$
(2.26)

The $i_{dc}(t)$ can be separated as a DC component, i_{dc} and an AC component, $i_{dc,ripple}(t)$.

Then the double-line frequency component can be extracted such that:

$$V_{dc}^{n}i_{dc,ripple}(t) \cong S\cos(2\omega_{g}t - \partial)$$
(2.27)

Rearranging the above equation yields:

$$i_{dc,ripple}(t) = \frac{S}{V_{dc}^n} \cos(2\omega_g t - \partial) = I_{dc,ripple} \cos(2\omega_g t - \partial)$$
(2.28)

Then the capacitance of the DC-link capacitor can be easily obtained given the magnitude of the maximum allowed ripple voltage, $V^{max}_{dc,ripple}$ [39], [40], [19], [20].

$$C_{dc} = \frac{I_{dc,ripple}}{2\omega_g V_{dc,ripple}^{max}} = \frac{S}{2\omega_g V_{dc}^n V_{dc,ripple}^{max}}$$
(2.29)

2.3.3 Switching Circuit Configuration

By selecting the full bridge configuration, the minimal allowed DC-link voltage can be set to be the peak value of the AC grid voltage. Thus, power MOSFETs, instead of higher voltage IGBTs, can beused as the switching devices which enables use of a high switching frequency (> 20kHz) without introduction of excessive switching loss. Furthermore, showing in Figure 2.8, using unipolar voltage switching scheme effectively moves the first major harmonic of the bridge output voltage from order (mf – 1) to the order of (2mf - 1), where mf is the frequency modulation ratio - the ratio between the switching frequency and the fundamental frequency. The output filter thus reduces its size for "free".



Figure 2.8: Generic DC-link voltage waveform

Since this full bridge configuration with SPWM unipolar voltage switching scheme is commonly used in voltage sourced inverters, further investigations will not be presented in this thesis. A full detail analysis can be found in [41].

2.3.4 Driver and isolation Switching Circuit

The bootstrap power supply is one of the most widely used methods to supply power to the high-side drive circuitry of a gate driver IC. The bootstrap power supply consists of a bootstrap diode and a bootstrap capacitor; this circuit is illustrated in Figure 2.9. This method has the advantage of being both simple and not expensive. However, the requirement to refresh the charge on the bootstrap capacitor may result in limitations on the power converter's duty-cycle and the power switch's on-time. One capacitor and bootstrap resistance selection can drastically reduce these limitations. The maximum voltage that the bootstrap capacitor (V_B) can reach is dependent on the elements of the bootstrap circuit shown in Fig. 2.9.

The voltage drop across R_B , V_d of the bootstrap diode, the drop across the low-side switch (V_{CEON} or V_d , depending on the direction of current flow through the switch), and if present, the drop across a shunt resistor placed between the low-side switch's emitter and the DC rail, all need to be considered. The intent of this document is to develop the bootstrap sizing theory and practice, while focusing in particular on topologies where the gate driver IC features the integrated the bootstrap "diode".



Fig 2.9 Bootstrap Driver Mosfet circuit

Two steps for this part included in these points:

- Determining bootstrap capacitance, CB-STRAP
- Determining bootstrap diode, D_{BS}, and resistor, R_C

These points are explained in the titles blow.

2.3.4 .1 Determining bootstrap capacitance, CB-STRAP

The charge of the bootstrap capacitor $C_{B-Strap}$ must be optimized to provide a sufficient power supply to the gate-drive opto-coupler in its smallest size. This helps to reduce cost, save board space and decrease charging time. The minimum size of $C_{B-Strap}$ needed to store enough charge for gate-drive operation can be calculated with the following equation:

$$C_{B-Strap} \ge 1.5 \left(\frac{Q_g + \frac{I_{CC} \times m}{f} + \frac{I_{BCS (LEAK)} \times m}{f}}{V_{ripple}} \right)$$
(2.30)

Where,

f = gate-drive PWM switching frequency

m = modulation index for PWM (duty cycle) of mosfet, Q1

 I_{CC} = gate-drive supply current

 Q_g = gate charge for mosfet, Q1

 $I_{BCS(LEAK)}$ = bootstrap capacitor leakage current

 V_{ripple} = maximum ripple voltage allowed

The pulse wide modulation switching frequency (PWM) mentions to the number of times per second that the bootstrap-powered gate drive requires to turn on and drive its MOSFET. Modulation index for PWM of the top-bridge MOSFET, Q1, refers to the duty cycle at which Q1 turns on in a particular time period. These parameters depend on the application and its design requirements. Gate charge of the upper MOSFET, Q1, refers to the amount of charges required at the gate of the MOSFET to turn it on. This parameter can be found in the MOSFET's datasheet. Bootstrap capacitor C_{BS} leakage current will happen if an electrolytic capacitor is used. This parameter can be found in the capacitor's datasheet, but can be ignored if other types of capacitors are used.

The factors relating to gate-drive opto-couplers that will affect the bootstrapping efficiency are I_{CC} and V_{RIPPLE} . Gate-drive supply current, I_{CC} , can be found in the gate drive's datasheet electrical specifications. TLP250 consumes a low maximum supply current of 2.5 mA, making it very efficient, since less power is needed for the opto-coupler while more can be delivered to drive the gate of the MOSFET.

The maximum ripple voltage allowed refers to the stability of the bootstrap power supply in order to provide an optimum MOSFET gate voltage, typically at 15 V. The TLP250 has a rail-to-rail output voltage which means the output does not suffer any drop from the supply, V_{CC} , applied to the gate-drive opto-coupler. This is unlike the older generation gate-drive opto-couplers which suffer a $3V_{BE}$ drop due to the bipolar Darlington output stage. In other words, the rail-to-rail output of the TLP250 will increase the bootstrap power supply ripple margin, which is inversely proportional to the size of the bootstrap capacitor. Hence, a smaller C_{BS} can be used without concern that the V_{CC} will fall below the MOSFET's optimum gate voltage.

2.3.4.2 Determining bootstrap diode, D_{BS} , and resistor, R_c

The fast recovery diode it is recommended for bootstrap circuit , D_{BS} , be selected to minimize the amount of leakage charge flowing back from C_{BS} into the V_{CC} supply. The

maximum reverse recovery time specification, t_{rr} , can be found in the diode's datasheet. The R_{BS} resistor is used to limit the surge current through the diode and to the V_{CC} pin of the gatedrive opto-coupler, the diode MUR140 has been selected.

To select the maximum value of R_{BS} , the $C_{BS} \times R_{BS}$ time constant must be able to meet the minimum charging time.

An R_{BS} value that is too high will not allow sufficient time for the bootstrap capacitor C_{BS} to charge to the required V_{CC} voltage. The maximum R_{BS} value is given in the following equation:

$$R_{BS} \le \left(\frac{\frac{1}{f} \times (1-m)}{C_{BS}}\right) \tag{2.30}$$

2.4 Output Filter Design

After the designing the fundamentals parts, the output filter design is necessary for the grid connected inverter's ,to meet the aforementioned harmonic reduction target, third order LCL filter, Figure 2.10, was used. A switching frequency of 20 kHz was selected based on considerations for the filter size and the practical implementation of the digital controller. $V_t(t)$ stands for the terminal voltage or the output voltage of the full bridge inverter, which consists of a fundamental component and higher order harmonics components.



Figure 2.10 Output LCL filter of the inverter

Solving the grid current in Laplace domain using superposition yields the following transfer functions:

$$\frac{I_g(s)}{V_t(s)}\Big|_{V_g=0} = -\frac{sC_f R_d + 1}{s^3 L_i L_g C_f + s^2 C_f R_d (L_i + L_g) + s(L_i + L_g)}$$
(2.31)

$$\frac{I_g(s)}{V_g(s)}\Big|_{V_t=0} = -\frac{s^2 L_i C_f + s C_f R_d + 1}{s^3 L_i L_g C_f + s^2 C_f R_d (L_i + L_g) + s(L_i + L_g)}$$
(2.32)

From the above Equation (2.31) and (2.32), one can observe that the grid current Ig(t) depends on both the terminal voltage $V_t(t)$ and the grid voltage $V_g(t)$. As discussed before, the output filter design will not take harmonic grid voltage distortion into consideration because IEEE-1547 allows the presence of harmonic current distortion caused by grid voltage distortion. Therefore, Equation (2.32) will not be taken into consideration in output filter design.

The terminal voltage $V_t(t)$ contains a fundamental component and higher frequency components which could result in higher frequency distortions on the grid current $I_g(t)$ Therefore, Equation (2.31) is used as the output filter transfer function as:

$$H_f(s) = \frac{I_g(s)}{V_t(s)}\Big|_{V_g=0} = -\frac{sC_f R_d + 1}{s^3 L_i L_g C_f + s^2 C_f R_d (L_i + L_g) + s(L_i + L_g)}$$
(2.33)

The RMS value of the higher order frequency components of $V_t(t)$ can be calculated using the look up table from [41] (refer to Appendix B), given the nominal DC-link voltage V_{dc}^n :

$$\left|V_t(jh\omega_g)\right| = \frac{1}{\sqrt{2}} \cdot 2 \cdot \frac{(\hat{V}_{Ao})_h V_{dc}^n}{V_{dc}^n} = \frac{1}{\sqrt{2}} \cdot k(h) V_{dc}^n$$
(2.34)

The $(\hat{V}_{Ao})_h$ is the peak value of each harmonic voltage between one leg of the bridge and the centre point of the DC-link, $V_{Ao}(t)$. In full bridge configuration, $v_t(t) = 2v_{Ao}(t)$.

 $k(h) = \frac{(V_{Ao})_h}{\frac{1}{2}V_{dc}^n}$ is tabulated as a function of ma and the orders of harmonics (refer to Appendix B for details about the harmonics table). Therefore, combining (2.33) and (2.34), the RMS value of the harmonic current can be expressed as:

$$\left|I_g(jh\omega_g)\right| = \frac{1}{\sqrt{2}} \cdot \left|H_f(jh\omega_g)\right| \cdot k(h) \cdot V_{dc}^n$$
(2.35)

Remember that $|Ig(jh\omega_g)|$ can not exceed 0.3% of the rated current of the inverter. Therefore, given the RMS value of the rated grid current Irated g the following relationship can be derived:

$$\frac{|H_f(jh\omega_g)|\cdot k(h)\cdot V_{dc}^n}{\sqrt{2}\cdot I_g^{rated}} < 0.3\%$$
(2.36)

Rewrite for $|\mathbf{H}_f(jh\omega_g)|$, then

$$\left|H_f(jh\omega_g)\right| < \frac{0.3\%\sqrt{2} \cdot I_g^{reted}}{V_{dc}^n \cdot k(h)}$$
(2.37)

Given from Appendix B, the worst case k(h) at (2mf - 1) is 0.37. Then, substituting the parameters from the inverter specification and using a switching frequency of 20 kHz, we get the magnitude of the filter transfer function $|\text{Hf}(jh\omega_g)|$ at (2mf - 1):

$$\left|H_f\left(j\left(377(2m_f-1)\right)\right)\right| = \left|H_f\left(j(376614)\right)\right| = \frac{0.3\%\sqrt{2}\cdot27A}{400V\cdot0.37} = -189 \ dB \tag{2.38}$$

With the transfer function of the filter derived in Equation (2.33), at $\omega = 376614$, the magnitude of H_f (j376614) from the magnitude plot of H_f (j ω) should at most be -189dB. This is the guideline of choosing the values for L_i, L_g, C_f and R_d.

2.5 Components for the implementation:

After all design and calculations to chosen the optimum components parameters in previous sections, the input filter, flyback DC/DC converter, H-bridge inverter and output filter components are shown in the table 2.3 below. This table shown the name of components, parameters of each component designed, and the best reference component existing in the market (electronic stores).

<u>N°</u>	<u>Components</u>	<u>Parameters</u>	<u>References (market)</u>	<u>Stage</u>
1	Input capacitor Cpv	2000uF, 63v	2200uF, 63v	Innut Filter stage
2	Input indictor Lpv	24uH/27A	//	input i nter stuge
3	Primary indictor Lp	180 uH/27A	//	
4	Number Turns N1	15	//	
5	N2/N1	9	//	
6	Wire Diameter	6mm ²	6 * 1 mm ²	
7	Transformer core	55mm*45mm*16mm	EE55	
8	Ae Transformer	4900nH	//	
9	gab Transformer	1.2 mm	//	
			MUR1640	Flyback stage
10	Output Diodes fluback	4A, 500V	(16A,600V)	
11	Switch flyback	Mosfet 27A,500v	2 X IRFP460	
12	Driver Switch Flyback	Driver high side min 12 v	TLP250 (Vb=32 V)	
13	Capacitor bootstrap flyback	1uF,25V	1uF,25V	
14	Resistor bootstrap flyback	10Ω, 0.25w	10Ω, 0.25w	
		High speed		
15	Diode bootstrap flyback	diode,0.2A,25v	MUR140	

TABLE 2.3 The components of proposed prototype grid connected PV inverter.

16	Resistor gate switch Flyback	22Ω, 0.25w	22Ω, 0.25w	
17	Capacitor Snubber flyback Csn	0.22uF, 1000 V	0.22uF, 1000 V	
18	Resistor Snubber flyback Rsn	45Ω, 2w	47Ω, 2w	
19	DC Link Capacitor Cdc	450 uF, 400V	450 uF, 400V	
20	Switch's Inverter	Mosfet 5A,500v	7N65 (7A,650V)	
21	Capacitor Snubber Inverter Csnv	0.056uF, 1000 V	56nF, 1000 V	
22	Resistor Snubber Inverter Rsnv	12Ω, 2w	12Ω, 2w	
		Driver high side Vbmin 12		
23	Driver switch's	v	TLP250 (Vb=32 V)	Inverter stage
24	Capacitor bootstrap Inverter	10uF,25V	10uF,25V	
25	Resistor bootstrap Inverter	2.2Ω, 0.25w	2.2Ω, 0.25w	
		High speed		
26	Diode bootstrap Inverter	diode,0.2A,25v	MUR140	
27	Resistor gate switch Inverter	22Ω, 0.25w	22Ω, 0.25w	
28	Indictor filter Li	400uH		
29	Indictor filter Lg	250uH		Output Filter
30	Capacitor filter Cf	30uF/400v	56uF/400v	Stage
31	Resistor filter Rd	2Ω,5w	2Ω,5w	

Conclusion

In this chapter, the design of all components of the grid connected PV inverter has been presented in detail, with the flyback system and the H-bridge inverter being presented for different operational situations. The flyback system was chosen for deployment within the DC/DC converter because this stricture is very well adapted for use within the grid connected PV inverter model. The structure of H-bridge inverter for the DC/AC part has been chosen and is shown in conjunction with a fully incorporated low pass filter (LPF) at the inverter output. The last table in this chapter illustrates all components of grid connected PV inverter for implementation directly in next chapters.

Chapter 3

Controller of the PV-Inverter

Introduction	
3.1 Control of Flyback converter	58
3.1.1 Maximum Power Point Tracker (MPPT)	60
3.1.1.1 Perturb and Observe method	61
3.1.1.2 Incremental Conductance method	62
3.1.1.3 Parasitic Capacitance method	63
3.1.1.4 Constant Voltage method	64
3.1.1.5 Constant Current method	64
3.1.2 Proposed Algorithm Variable Step Size IC MPPT (VSS IC)	64
3 .2 Control of H-bridge Inverter	70
3.2.1 DC-Link Controller	70
3.2.2 Grid Synchronization and current control	74
3.2.3.1 Sinusoidal pulse width modulation (SPWM)	74
3.2.3.2 SPWM with bipolar voltage switching	75
3.2.3.3 SPWM with unipolar voltage switching	76
Conclusion	

Introduction

Current PV systems are faced with many challenges, these include, low efficiency, high cost and the problem of the power maximization. To address some of these issues the following chapter we presents a new and novel algorithm to track the maximum power point applied to the DC/DC flyback converter. Further to this a PWM control method for the H-bridge inverter is implemented as well as a DC-link voltage controller and a Phase Locked Loop (PLL) to track the fundamental component of the grid voltage and grid current controller using the Hbridge inverter. A simplified diagram illustrating these techniques is shown in Figure 3.1.In this chapter there are two fundamental sections, the first section discussed the controller of the DC/DC or Flyback converter and the second section adapts this technique for use with the DC/AC or H-bridge inverter.



Fig 3.1 The controllers of PV inverter

In this chapter there are two fundamental parts, the first part talking about the controller of the DC/DC or Flyback converter, the second part the same first but for DC/AC or H-bridge inverter.

3.1 Control of Flyback converter

In the PV systems, the converter DC/DC is very important for getting the maximum power, there are many technics for tracking this power, and the very important parameters to execute these technics are the inputs values of the voltage and the current. The inputs of the controller are the measured output voltage and current of the solar panel. This value is not the actual value of the output voltage and current, but the actual value has been converted to a value

between 0 and 5 V. Based on these inputs voltage and current, the algorithm performs its calculations. The output of the controller is the adjusted duty cycle of the PWM, which drives the DC-DC (Flyback) converter's switching device. A different duty cycle causes a different operating point.



Flyback Controller

Fig 3.2 Design the controller of Flyback converter

Any converter controller is required three fundamental functions :

- The analog to digital converter
- The algorithm
- The output generator PWM are all required functions
 This is shown in the previous figure 3.2, and explained in the next titles.

Analog to Digital Converters

The function of the Analog to Digital Converter (ADC) is to measure the input signals of the controller, which are between 0 and 5 V, that represents the output voltage and current of the solar panel and convert them into binary numbers with which the controller can perform its calculations [40]. These measurements and conversions should be as accurate as possible, as inaccurate measurements and conversions could lead to inaccurate tracking of the optimal voltage to get the maximum power.

> Algorithm

The major function of the controller is performing the calculations to find the next operating duty cycle. The inputs of this process are the binary numbers provided by the ADCs, those

binary numbers represent the solar panel's output voltage and current [40]. Based on the algorithm calculations, the controller output should be a signal which tells the PWM generator the value of the duty cycle.

PWM Generator

The input of the Pulse Wide Modulation generator module is the needed duty cycle of the PWM signal. Based on this input, the PWM generator creates a PWM signal with this desired duty cycle and this PWM signal is subsequently sent to the switching device of the flyback converter.

3.1.1 Maximum Power Point Tracker (MPPT)

Maximum power point tracking (MPPT) algorithms present the theoretical means to get the MPP of PV cells; these algorithms can be realized in many different forms of hardware and software. This is a technique used to obtain the maximum possible power from a varying source. In photovoltaic systems the I-V curve is non-linear, thereby making it difficult to be used to power a certain load. This is done by utilizing a boost converter whose duty cycle is varied by using a MPPT algorithm. Few of the many algorithms are listed below [41], [42], [43] and [44].



Fig. 3.3 General block diagram of PV system with MPPT.

A flyback converter is used on the load side and a solar panel is used to power this converter. The principal parameters are short-circuit current, Isc and open circuit voltages, Voc as illustrated

on the Fig.3.4 are specified in the PV module data sheet of attached to it. The values are at standard test condition (STC) and they are called PV performance parameters.



Fig.3.4: Current, Voltage and Power characteristics of a PV module [45]

In the photovoltaic systems there are many methods used for maximum power point tracking a few are listed below:

- Perturb and Observe method
- Incremental Conductance method
- Parasitic Capacitance method
- Constant Voltage method
- Constant Current method

These methods are explained in the next points.

3.1.1.1 Perturb and Observe method

The P&O method is the most common. In this method very less number of sensors are utilized [43] and [46]. The algorithm changes the operating voltage in the required direction and samples dP/dV. If dP/dV is positive, then the algorithm increases the voltage value towards the MPP until dP/dV is negative. This iteration is continued until the algorithm finally reaches the MPP. This algorithm is not suitable when the variation in the solar irradiation is high. The voltage never actually reaches an exact value but perturbs around the maximum power point (MPP) with fixed step. The flowchart of P&O MPPT algorithm is shown in Fig. 3.5.



Fig 3.5 Flowchart of the P&O MPPT algorithm.

3.1.1.2 Incremental Conductance method

Interest of photovoltaic energy in electrical power applications has greatly increased. However, it still has relatively low conversion efficiency. Therefore, efficiency improvement can be done using high efficiency power trackers which are designed to extract the maximum possible power from the PV system (maximum power point tracking MPPT), the PV system with MPPT is shown in Fig.3.3 Many MPPT techniques have been proposed, the Incremental Conductance method is often considered, due to its high performances such as easy implementation, high tracking speed and better efficiency. This method focuses directly on power variations which the conductance and the incremental conductance of the PV panel are calculated instantaneously, increasing on the left of the MPP and decreasing on the right hand side of MPP. The maximum power point (MPP) is obtained when the derivative of PV powerby the voltage(dP/dV) is zero. The basic equations of this method are as follows:

$$\frac{dP}{dV} = 0 \tag{3.1}$$

Equation (5) can be rewritten as:

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V \frac{d(I)}{dV} = 0$$
(3.2)

$$\frac{dI}{dV} = -\frac{I}{V} \text{ at MPP}$$
(3.3)

$$\frac{dI}{dV} > -\frac{I}{V} \text{ at left of MPP}$$
(3.4)

$$\frac{dI}{dV} < -\frac{I}{V} \text{ at right of MPP}$$
(3.5)

The flowchart of the Incremental Conductance method is illustrated in Fig.3.6



Fig 3.6 Flowchart of the IC MPPT algorithm.

3.1.1.3 Parasitic Capacitance method

This method is an improved version of the incremental conductance method, with the improvement being that the effect of the PV cell's parasitic union capacitance is included into the voltage calculation [43] and [46].

3.1.1.4 Constant Voltage method

This method which is a not so widely used method because of the losses during operation is dependent on the relation between the open circuit voltage and the maximum power point voltage. The ratio of these two voltages is generally constant for a solar cell, roughly around 0.76. Thus the open circuit voltage is obtained experimentally and the operating voltage is adjusted to 76% of this value [44].

3.1.1.5 Constant Current method

Similar to the constant voltage method, this method is dependent on the relation between the open circuit current and the maximum power point current. The ratio of these two currents is generally constant for a solar cell, roughly around 0.95. Thus the short circuit current is obtained experimentally and the operating current is adjusted to 95% of this value [44].

The methods have certain advantages and certain disadvantages. Choice is to be made regarding which algorithm to be utilized looking at the need of the algorithm and the operating conditions. For example, if the required algorithm is to be simple and not much effort is given on the reduction of the voltage ripple then P&O is suitable. But if the algorithm is to give a definite operating point and the voltage fluctuation near the MPP is to be reduced then the IC method is suitable, but this would make the operation complex and more costly.

3.1.2 Proposed Algorithm Variable Step Size IC MPPT (VSS IC)

To optimize the efficiency of large photovoltaic modules; maximum power point tracker algorithm (MPPT) is required. In this context, a large number of MPPT methods have been developed and improved [47, 51-58]. These techniques vary in complexity, accuracy, and speed, oscillation around the MPP, hardware implementation sensor requirement, [77, 59]. The widely MPPT techniques are: the perturbation and observation (P&O) algorithm [59-61], Incremental Conductance (IC) method [47, 52, 56, and 62] and Hill Climbing (HC) [63-65]. For faster and more accurate MPPT controllers using neural network, fuzzy logic, particle swarm optimization (PSO) based MPPT and genetic algorithms have been proposed [66]. Despite these methods have a good performance in dealing with the nonlinear characteristics of the I–V curves, they require extensive computation the versatility of these methods is limited [58,66].

The perturbation and observation P&O, Incremental Conductance (IC) and Hill Climbing (HC) methods based on fixed iteration step size are simple and have good performances. However, they are characterized by slow convergence; oscillations in the PV power around

the MPP, operation fail under rapidly changing atmospheric conditions, using small perturbation step size, oscillation can be reduced, but the speed of tracking MPPs will be slower. To acquire a fast response speed and overcome the aforementioned drawbacks, a modified MPPT algorithms with variable step size have been the subject of many investigations [47,63,66-67], which the step size is automatically adapted according to the derivative of power to voltage (dP/dV) of a PV panel.

In general, the conventional IC MPPT algorithm uses a fixed step size to track the maximum power point (MPP). Thus the tracking speed and accuracy are highly depending on the fixed step size: The extracted power from the PV array using a large step size contributes to faster dynamics, but increases the losses in steady state due to large perturbations around the MPP, using small perturbation step size, oscillation can be reduced, but the tracking speed will be slower. Thus, the corresponding design should satisfactorily address the trade-off between the dynamics and steady state oscillations.

A large number of variable step size Incremental Conductance MPPT algorithm with direct control have been proposed and investigated [48,51,57,68-71], In which the step size is automatically adjusted according to the first derivative of power with respect to voltage (dP/dV),to current (dP/dI) or (dP/dD) [48,51,57,58,68]. The variable step size Incremental Conductance MPPT algorithms are mostly similar to the conventional incremental conductance and the only difference is the step size calculation, a constant value N is often multiplied with the derivative (dP/dV, dP/dI, dP/dD).

Kok Soon et al [48] introduced new tracking steps to identify the changes in solar irradiation level using the variations in current (dI) and voltage (dV) of the PV module instead of the slope (dP/dV) of the P–V curve. Fangrui et al. [58], Ahmed, Emad et al. [64], Abdourraziqet al. [24] and Rahman et al. [70], proposed new variable step size IC MPPT, in which, the fixed step size is multiplied with the slope of the P–V curve.

In Ref [57], Pandey et alused the derivative (dP/dD) as the variable step size, the scaling factor is tuned at design time to adjust the step size, which is proportion to dP/dV term.

In ref [52], Qiang et alused the derivative of power to current (dP/dI) to determine the variable increment for the IC MPPT algorithm. Comparison of common variable step size Incremental Conductance MPPT with direct control is summarized in Table. 1.

In addition, to improve the efficiency of PV systems, many DC/DC converters have been used in PV systems, a Flyback converter is one of the common topologies considered for PV modules since is an isolated power converter through transformer and it provides a simple topology, low cost, reduced number of semiconductor switches, operate over wide range of input voltage variation, capable of achieving the optimal operation regardless of the load value [72-73].



Fig. 3.7 Fixed and variable step size MPPT operation.

In general, the conventional IC MPPT algorithm uses a fixed step size to track the maximum power point(MPP). Thus the tracking speed and accuracy are highly dependent on the fixed step size. The extracted power from the PV array using a large step size contributes to faster dynamics, but increases the losses in steady state due to large perturbations around the MPP, using small perturbation step size, oscillation can be reduced, but the tracking speed stays slower. Thus, depending on each operational condition, the corresponding design should satisfactorily address the trade off between the dynamics and steady state oscillations as shown in previous Fig.3.7.

In this paper, a new variable step size Incremental Conductance MPPT algorithm with direct control has been proposed. Modeling and analysis of different operational conditions of Incremental Conductance method have been presented. The proposed variable step size and fixed step size IC MPPT methods are tested and validated using Matlab/Simulink model and experimental prototype MPPT system was developed, using Flyback converter, which is controlled by control circuit based on Dspic30F4011. The different aspects of the system and parameters have been implemented. A comparative study between the proposed variable step size and fixed step size IC MPPT method under similar operating conditions is presented. Many efficiency parameters have been suggested: tracking accuracy, response time, ripple, and duty cycle oscillations.

As mentioned before, the conventional MPPT methods based on fixed step size has a good performance. However, they are characterized by slow convergence; oscillations in the PV power around the MPP,operation fail under rapidly changing atmospheric conditions and they can get lost and track the MPP in the wrong direction during rapidly changing atmospheric conditions. Speedy tracking can be achieved with larger step size but excessive steady state oscillations is unavoidable, smaller step size can reduces the oscillations with slower dynamics. Solving these dilemmas, many contributions have been introduced using variable step size and significant progress has been made, where the algorithm changes the step size automatically according to the PV array characteristics [77, 47, 54, 62]; depending on each operational condition, step size should make a satisfactory tradeoff between the dynamics and oscillations. Therefore, from the basic principle of MPPT, this paper proposes a new variable step size IC MPPT algorithm, which it's characterized by more simplicity, faster response time and less oscillations. The flowchart of variable step size IC MPPT algorithm is shown in Fig. 3.8.

	Left MPP		At MPP	Right MPP	
Variable step size N* dP/dV - dI	Far the MPP Large step size	Near the MPP Small step	0	Near the MPP Small step	Far the MPP Large step

Table2 Principle of proposed variable step size ICMPPT method.

			not be	efore the			g factor N
Notes	Good dynamic performance Medium tracking rapidity No steady state oscillation High Overshoot Scaling factor N is calculated	Good dynamic performance No steady state oscillation High Overshoot Medium tracking rapidity	high steady state oscillation high Overshoot scaling factors M is chosen, it can changed in the tracking process	Multiple value of N Too slow high steady state oscillation ,there available maximum power has be reduced	Good dynamic performance No steady state oscillation, Important Overshoot	High Response time High Ripple Important Overshoot	Good tracking rapidity Good accuracy No steady state oscillation No Overshoot Less duty cycle oscillations Scalin, is adjusted manually
Controller implementation	TMS320LF2407 DSP	C515C microcontroller	TMS320F2808	PIC18F4520	Microchip PIC18F4520	Only simulation	dsPlC30F4011
DC/DC ©nverter	Push-pull converter	Boost converter	Boost converter	Buck converter	SEPIC converter	Boost converter	Flyback converter
Variable step	$D(k) = D(k - 1) \pm N^* \left \frac{dP}{dV} \right $	$C = P^{\Pi_{\otimes}} dP dI $	$D(n) = D(n-1) + M^* e(n) e = \frac{dV}{dl} + \frac{V}{l}$	$step = N^* \frac{dP}{dV}$	$step = N^*abs(\frac{dP}{dV})$	$D(n) = D(n-1) \pm N^* \frac{ dP }{ dV }$	$D(k) = D(k-1) \pm N^* \frac{dP}{dV - dT}$
Publication year	2008	2011	2011	2013	2014	2014	2015
Authors	Liu et al.	Mei et al.	Ahmed Emad et al.	Rahman et al.	Tey and Mekhilef	Abdourraziq et al.	Proposed
Ref							

TABLE I

Comparison of common variable step size Incremental Conductance MPPT with direct control

[67,61,76,75,53,74]

The variable step size method proposed is given as follows:

$$D(k) = D(k-1) \pm N * \left| \frac{dP}{dV - dI} \right|$$
(3.6)

where D(k) and $D(k_1)$ are the converter duty cycle at the instant (k) and the converter duty cycle at the previous instant(k_1). N is the scaling factor adjusted at the sampling period to regulate the step size , which is manually adjusted. dI, dV and dP are the PV array output current derivate, voltage derivate and power derivate respectively. They can be formulated by:

$$dI(k) = I(k) - I(k-1)$$
(3.7)

$$dV(k) = V(k) - V(k-1)$$
(3.8)

$$dP(k) = P(k) - P(k - 1)$$
(3.9)

where: I(k), V(k) and P(k) are the PV array output current, voltage and power at the instant(k) $I(k _1)$, $V(k _1)$ and $P(k _1)$ are the PV array output current, The basic principle of the proposed variable step size is illustrated in Table.2:



Fig. 3.8. Flowchart of the variable step size IC MPPT algorithm.

In order to complete controller of the PV inverter, the next section will be design the controller for the H-bridge inverter.

3.2 Control of H-bridge Inverter

This part discusses different techniques for switching and controlling of the H-bridge power stage. Methods to switch voltage sources inverter (VSI) have been explained and presented, the deferent control parts presented in the figure 3.9 blow.



Fig 3.9 Deferent control parts of the H-Bridge inverter

There are many points are necessary for controlling the Grid connected H-bridge inverter:

- DC-Link Controller
- Grid Synchronization and current control
- Generations of signals PWM

These points are explained in titles below:

3.2.1 DC-Link Controller

The aim of the DC-link controller is to control the average value of the DC-link voltage. Figure 3.10 is a simplified power stage diagram which is used to analyze the DC voltage behaviour.


Figure 3.10: Inverter power stage diagram [78]

In the DC side The differential equation is[78]:

$$C_{dc} \,\frac{dv_{dc}(t)}{dt} = i_{dc}(t) \tag{3.10}$$

 $i_{dc}(t)$ consists of two components, a DC component, Idc and a double-line frequency AC component, $i_{dc,ripple}$ (t). Both of them can be obtained from the power balance equation [78]:

$$v_{dc}(t)i_{dc}(t) = \hat{V}_g \cos(\omega_g t) \hat{I}_g \cos(\omega_g t - \emptyset)$$
(3.11)

$$v_{dc}(t)I_{dc} + v_{dc}(t)i_{dc,ripple} = \frac{\hat{V}_g \hat{I}_g}{2} \cos \emptyset + \frac{\hat{V}_g \hat{I}_g}{2} \cos \left(2\omega_g t - \emptyset\right)$$
(3.12)

From equation (3.16), the two components of the DC current can be expressed as:

$$I_{dc} = \frac{\hat{V}_g}{2v_{dc}(t)} \hat{I}_g \cos \phi = \frac{V_g^{rms}}{\sqrt{2}v_{dc}(t)} \hat{I}_g \cos \phi$$
(3.13)

$$i_{dc,ripple}(t) = \frac{\hat{v}_g \hat{l}_g \cos\left(2\omega_g t - \emptyset\right)}{2v_{dc}(t)}$$
(3.14)

Since we align the parallel component of the current reference signal with the grid voltage using a grid synchronization function block, the grid current $i_g(t)$ has its parallel component aligned with the grid voltage as shown in the phasor digram in Figure 3.11.



Figure 3.11: Phasor diagram of i_g and its two components

Consequently, Equation (3.17) can be rewritten to be

$$I_{dc} = \frac{V_g^{rms}}{\sqrt{2}v_{dc}(t)} \hat{I}_{g\parallel}$$
(3.15)

Then, we linearize these parameters to about the nominal grid voltage V_g^n and nominal DC voltage V_{dc}^n [79]:

$$I_{dc} = \frac{V_g^n}{\sqrt{2}V_{dc}^n} \hat{I}_g \|$$
(3.16)

after that, the complete model of the voltage loop can be drawn and is shown in Figure 3.12. A notch filter, $H_n(s)$, has a form of Equation (3.17) is applied to the voltage loop to filter out the double-line frequency current ripple component idc,ripple(t) because the double-line frequency ripple current produces a double-line frequency ripple voltage on the DC-link [78].

$$H_{notch} = \frac{s^2 + 2\sigma_1 \omega_n s + \omega_n^2}{s^2 + 2\sigma_2 \omega_n s + \omega_n^2}$$
(3.17)

This is undesirable because this ripple signal would couple through the voltage controller and cause undesirable high frequency component would appear on the current reference signal of the current control loop, Figure 3.13.



Figure 3.12: Voltage loop of the H-bridge inverter



Figure 3.13: Effect of the double-line frequency ripple on the current reference signal[78]

Where:

 ω_n is twice the fundamental frequency.

 σ_1 is chosen to be 0.008 and σ_2 is chosen to be 1.

The "current synchronization" block in the diagram is the part that the parallel current reference, which is generated from the voltage controller, is converted to a grid synchronized sinusoidal signal. The current loop, $G_c(s)$ has a form of [80]:

$$G_{c}(s) = \frac{G_{i}(s)G_{f}(s)}{G_{i}(s)G_{f}(s)-1}$$
(3.18)

Where:

- $G_i(s)$ is the PR controller from the current loop.
- $G_f(s)$ is the plant model derived in Equation (3.2).

A simple PI controller is used as the DC voltage loop compensator, which has the form of [78] [80]:

$$G_{\nu}(s) = K_{p}^{\nu} + \frac{K_{i}^{\nu}}{s}$$
(3.19)

3.2.2 Grid Synchronization and current control

Once the $v_{g\parallel}$ and $v_{g\perp}$ are obtained from the grid voltage estimator, and \hat{V}_g is obtained from the amplitude identifier, the control of the phase of the synchronized current reference becomes possible. Therefore, given the grid reference current's parallel and orthogonal components, $i_{g\parallel}^{ref}$ and $i_{g\perp}^{ref}$, a synchronized current reference signal can be obtained by the following equation [81]:

$$i_{g}^{ref} = \frac{i_{g\parallel}^{ref} v_{g\parallel} + i_{g\perp}^{ref} v_{g\perp}}{\hat{V}_{g}}$$
(3.20)

Since the parallel component of the current reference $i_{g\parallel}^{ref}$ is aligned with the grid voltage, this part of the current then controls the active power flow to the grid. On the other hand, since the orthogonal component of the current reference $i_{g\perp}^{ref}$ is 90° leading the grid voltage, this part of the current controls the reactive power flow to the grid. Therefore, the input $i_{g\perp}^{ref}$ and $i_{g\parallel}^{ref}$ are the input control commands for the active and reactive power.

3.2.3 Generations of signals PWM

There are many techniques have been mentioned in [39] to control voltage source, VSI power stage. There are three major output current control techniques for the single phase which includes hysteresis band, predictive, and sinusoidal pulse width modulation control. This part will travel around different techniques of PWM and focus on the one that will appear to be the better in the control of the H-bridge inverter. The DC-AC inverters typically work on Pulse Width Modulation technique, this technique is a very advance and helpful technique in which width of the gate pulses are controlled by many methods. PWM inverter is used to stay the output voltage of the inverter at the rated voltage irrespective of the load. With pulse width modulation control, inverters usually switch between different circuit topologies, which mean that inverter is a nonlinear, specifically piecewise smooth system. In addition to this, the control strategies used in the inverters are also similar to those in DC/DC converters [82]. Pulse Width Modulation is a technique which is characterized by the generation of constant

amplitude pulse by modulating the pulse duration by modulating the duty cycle [83] [82] [84]. Analog PWM control requires the generation of both reference and carrier signals that are feed into the comparator and based on some logical circuit. The reference signal is the desired signal output maybe sinusoidal or square wave, while the carrier signal is either a saw tooth or triangular wave at a frequency significantly greater than the reference signal [83] [82]. Inverters DC/AC that use PWM switching techniques have a DC input voltage that is usually constant in scale. The inverters work is to take this input voltage and convert to the output AC where the scale and frequency can be controlled by this technique. In this area there are many different ways that pulse-width modulation can be implemented to shape the output to be AC power. These different types of PWM switching techniques have been discussed so far in [39] [83] [82].

The types of deferent PWM technics are:

- Sinusoidal pulse width modulation (SPWM)
- SPWM with bipolar voltage switching
- SPWM with unipolar voltage switching

These types are explained in the next titles:





Fig. 3.14: Comparison of desired frequency and triangular waveform [83] [84]

Pulse-width modulation (PWM), or pulse-duration modulation (PDM), this technique there are multiple numbers of output pulses per half cycle and pulses are of many different width.

The width of each pulse is varying in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The output signals are generated by comparing a sinusoidal reference signal with a high frequency triangular signal [83] [82]. This comparison of waveforms produces the SPWM signals to turn on/off switches. The sinusoidal reference signal frequency determines the frequency of the inverter. SPWM generating techniques have discussed in [83] [82] [84].

The modulation ratio or modulation index as explained in [83] [84] as the ratio of the amplitudes of the control voltage and triangle voltage. The modulation can also be in terms of frequencies ratios, termed as frequency modulation ratio. Modulation index controls the amplitude of the output voltage. Over modulation can cause large AC magnitude voltage even though the spectral content of the voltage is poor. In addition to that, in over modulation the output voltage has more harmonic contents. This type is shown in figure 3.14.

3.2.3.2 SPWM with bipolar voltage switching

In this type the switches are treated as two switch pairs [83] [84]. The fundamental idea is explain in [83] as the comparator is used to compare between the reference voltage waveform with the triangular carrier signal and produces the bipolar switching signal.



Fig.3.15: Bipolar SPWM switching and Pulse width modulation [83] [84]

When this signal applied to the switches of a single phase full bridge DC-DC the output in the two legs are equal but differ in polarity [83] [84]. The output voltage is determined by comparing the control signal and the triangular signal as shown in Fig 3.15 to get the switching pulses for the switching devices. The output of the switching patterns containing the fundamental frequency voltage. The detailed analysis of harmonics contents is explained in details in [84]. The resulting switching signal is seen in Fig 3.15.

3.2.3.3 SPWM with unipolar voltage switching

Unipolar PWM switching is used in the inverter power stage designed in this thesis. the switches in the two legs of the H-bridge inverter presented in Fig 3.9 are not switched simultaneously. The basic idea to produce SPWM with unipolar voltage switching is shown in Fig. 3.16. The different between the SPWM with bipolar voltage switching generators is that the generator uses another comparator to compare between the inverse reference waveform with the triangle voltage [83].



Fig.3.16: Unipolar Voltage switching Generation [83]

As pointed out in [84] it is similar that when the upper switches (S11 and S21) or (S12 and S22) are on the output voltage is zero. The switching scheme is shown in Fig 3.17, when the switching occurs the output voltage changes between zero and Vdc or zero and –Vdc voltage levels. This is why it is called SPWM with unipolar voltage switching.

The effective switching frequency is seen by the load is doubled and the voltage pulse amplitude is halved. Due to this, the harmonic content of the output voltage waveform is reduced compared to bipolar switching [85], [86], [87].

In this type [83] the effective switching frequency is seen by the load is doubled and the voltage pulse amplitude is halved. Due to this, the harmonic content of the output voltage waveform is reduced compared to bipolar switching. In unipolar voltage switching scheme the amplitude of the significant harmonics and its sidebands is much lower for all modulation indices thus making filtering easier, and with its size being significantly smaller. The SPWM unipolar voltage switching has the advantage of effectively doubling the switching frequency as far as output harmonics are concerned, comparing to bipolar voltage switching scheme. Also the voltage jumps in the output voltage at each switching are reduced to dV, as compared to twice d V in bipolar voltage switching. [83] [88] [84].



Fig. 3.17: Unipolar switching scheme [84]

Many advantages of SPWM with unipolar voltage switching mentioned in [39] [83] [84] made the power stage in this thesis to use this type of switching scheme. When used in full bridge converter the minimum DC link voltage will be seen to the output AC grid voltage. Thus, power MOSFETs, can be used as the switching device which enables use of a high switching frequency without introduction of excessive switching loss. For the harmonic analysis related to the switching scheme, sinusoidal pulse width modulation with unipolar switching scheme, changes the order of the major harmonic of the output voltage. Also the technique is very much commonly used in photovoltaic inverters [39].

Conclusion

A number of different and novel control methodologies for Grid connected PV-inverters have been studied and presented. Different maximum power point tracking techniques and a new algorithm featuring variable step size incremental inductance (VSS IC) has been presented for flyback control. Also several different types of the PWM and grid parameters control variants for the grid connected H-bridge inverter were discussed. All the control technics presented were validated by simulation and experimental testing as shown in the next chapter.

Chapter 04

Simulation and experimental validation for Grid connected PV- inverter

Introduction	81
4.1 Simulation results for Grid connected PV inverter	82
4.1.1 Flyback and new IC variable step size MPPT algorithm simulation	84
4.1.1.1 MPPT tracking	84
4.1.1.2 Response time	85
4.1.1.3 Duty cycle oscillations	86
4.1.1.4 Ripple	86
4.1.1.5 Overshoot	87
4.1.2 H-bridge Inverter simulation testing	87
4.1.2.1 H-bridge autonomy Inverter simulation	
4.1.2.2 Grid connected H-bridge inverter simulation	90
4.2 Experimental results for Grid connected PV inverter	92
4.2.1 Experimental results of the proposed variable step size IC MPPT	93
4.2.2 Experimental results of H-bridge inverter	86
Conclusion	99

Introduction

Developing the investigations into the power and control stages of the PV inverter discussed in the previous chapters, this chapter moves on to present the development of a complete prototype grid connected PV inverter. Divided into two sections the first discusses the simulation of the flyback converter and H-bridge inverter. This features a method that employs proposed variable step size and fixed step size IC MPPT methods and was tested and validated using Matlab/Simulink. Similarly the Flyback converter and H-bridge inverterwere validated and developed with Matlab/simulink modelling using the unipolar PWM control toolbox.In the second section of this chapter the testing the development experimental prototype PV inverter are discussed, developed and evaluated.



4.1 General view of grid connected PV inverter

The figure 4.1 shown the deferens parts we will discuss in the next sections, simulation section and also in the experimental section, all simulations and experimental results are commented.

4.1 Simulation results for Grid connected PV inverter

The PV inverter designed in this thesis as presented in figure 4.2. The inverter is designed based on the literatures discussed in previous chapters. The fixed voltage from the PV array is taken as 42V, which is assumed to be the only voltage available all the time at the PV arrays. The Flyback converter is used to amplify the voltage and to provide galvanic isolation between the PV array and the grid.

The DC-Link voltage is estimated to 325V that is enough to give the desired output AC voltage of 230V. The DC- bus voltage is maintained at the secondary of the transformer with turn ratio of 1: 9 and this will be controlled by the MPPT controller. The L-C-L output filter is designed to minimize the harmonics that present in the inverter output due to switching.



4.2 Simulation Models of PV inverter

In the following stages we will use the Matlab Models for flyback converter and the H-bridge inverter to get the simulation results. The first simulation section we will making the simulation for Flyback converter using the MPPT control to getting the maximum power, and also testing the new IC variable step size MPPT, this is studding in chapter three . In the second simulation section we will test the grid connected H-bridge inverter using the Unipolar PWM control to getting and discus the results.

4.1.1 Flyback and new IC variable step size MPPT algorithm simulation

One of the purposes of this thesis is to improve a model to test the dynamic performance of different MPPT algorithms. Detailed models of the PV system with the switching model of the power converter are computationally very heavy and the time that can be simulated in a normal computer is only a few seconds. However the simulation time required for testing the system with the irradiation profiles.

The algorithm proposed here was developed in Matlab®/Simulink® and consists of a model of the PV Module, which replaces the power converter. The proposed variable step size IC MPPT Control block generates the reference voltage using the MPPT algorithm under test. The model of the PV module used in this simulation was designed following the references [88]. This model shown in figure 4.3 below.



Figure 4.3 - Model used for simulations.

In another part the reference voltage generated by the MPPT Control block is converted to a current reference using the control scheme described in [88] and shown in Figure 4.4.



Figure 4.4 MPPT Controller.

The parameters of the system used in all the simulations performed in this thesis are as follows:

Solar panel characteristics at STC are shown in table 4.1 blow :

MSX-60
60 W
17.1 V
3.5 A
3.8 A
21.1
$-(80 \pm 10) mV/^{\circ}C$
(0.065 <u>+</u> 0.01)% °C
(−0.5 ± 0.05)% °C
47 ± 2 °C

Table 4.1 Electrical characteristics of Solarex MSX -60

Sampling frequency:

MPPT algorithm: 50 kHz

V and I measurements: 20 kHz

The characteristics of the solar module (MSX-60) were chosen in order to fulfil the requirements of the flyback converter, The sample frequency of the MPPT algorithm should not be very high because the dynamics of the weather conditions is slow compared to the dynamics of systems typically studied in control theory.

To illustrate the efficiency of the proposed variable step size ICMPPT method, a simulation and a comparative study between variable step size and fixed step size IC MPPT methods have been demonstrated, where the different aspects of the system and parameters have been implemented using Matlab/Simulink model.

A Flyback converter is used as the DC/DC converter interface between the PV array and the load to obtain the MPP. A 0.001 s sampling period is used for the MPPT algorithm. So, the duty cycle is updated every 0.001 s, the fixed step size is chosen to be 0.005, the scaling factor N is adjusted as 0.001.

Five improvements have been demonstrated such as:

- tracking accuracy
- ➢ response time
- ➤ duty cycle
- \succ oscillations
- ➤ ripple

The output power performance of variable step size and fixed step size IC MPPT method under insolation step change conditions are shown in the following figures:

4.1.1.1 MPPT tracking

Figure 4.5 shows maximum power point tracking variable step size and fixed step size IC MPPT methods corresponding to the input irradiation levels (1000, 700 and 500W/m), where we can see that both the MPPT algorithms discussed in this paper have considerable accuracy. The power values given by the proposed variable step size and fixed step size IC MPPT methods are very close to the theoretical value corresponding to irradiation levels.



Fig. 4.5. PV array output power with variable step size and fixed step size IC MPPT methods.

4.1.1.2 Response time

The maximum power point tracking comparison between variable step size and fixed step size IC MPPT methods is shown in Figure 4.6, the proposed algorithm shows a significant improvement in the response time. The energy lost can be reduced with variable step size IC MPPT method.



Fig. 4.6. PV array output power response time with variable and fixed step size IC algorithms.

From figures 4.7 and 4.8, where PV array output power due to sudden increase and decrease in irradiation is shown. It can be observed that the response time with variable step size IC MPPT algorithm are obviously better than this with fixed step size IC MPPT algorithm. Therefore, the proposed variable step size IC algorithm has a good tracking rapidity especially around the MPPT point.



Fig. 4.7. PV array output power due to sudden decrease in irradiation.



Fig. 4.8. PV array output power due to sudden increase in irradiation.

4.1.1.3 Duty cycle oscillations

From Figure 4.9, the results clearly illustrates that the variable step size IC MPPT method reaches the optimal duty cycle with less oscillations faster compared to the conventional fixed step size IC MPPT.



Fig. 4.9. Duty cycle for variable and fixed step size IC algorithms.

4.1.1.4 Ripple

From Figure 4.10, the improvement of variable step size IC MPPT method regarding ripple is undeniably clear.



Fig. 4.10. PV array output power ripple for variable and fixed step size IC algorithms.

4.1.1.5 Overshoot

From Figure 4.11, it can be observed that the overshoot due to irradiation changing from 1000W/m2 to 700W/m2 is less important in case of variable step size algorithm than in case of fixed step size.



Fig. 4.11. PV array output power overshoot for variable and fixed step size IC algorithms.

4.1.2 H-bridge Inverter simulation testing

These simulations will be described. It is worth to notice that a Matlab toolbox called Sim power system has been used. This software has been adopted because is very fast in simulating power electronics circuits.

Firstly we will simulate the H-bridge inverter without electrical grid then make semulation testing for grid connected H-bridge inverter, these simulations in the below titles.

4.1.2.1 H-bridge autonomy Inverter simulation

In this simulations will be described. It is worth to notice that a Matlab toolbox called Sim power system has been used. This software has been adopted because is very fast in simulating power electronics circuits.

The first simulation takes in account a single h-bridge connected to a resistive load. The output voltage have been calculated. In the figure 4.12 the block diagram of the analyzed circuit is shown.



Fig 4.12 MATLAB model of autonomy PV inverter.

In the PWM control there are two parts: one is used to create the PWM, while the other one generates the dead time. Within the H-bridge block, instead, the h-bridge itself and the load are present.

In the output inverter there is LC filter before the load, this filter used for amelioration the quality of output power or decrease the harmonics distortion value (THD).

The two due duty-cycles which drive the PWM generators are complementary. This means that when the signal related to the first duty-cycle is high, the signal referred to the other duty-cycle is low. In order to generate these duty-cycles, a division between a discretized reference voltage and the power supply voltage has been used.

The figure 4.13 shows how to make the duty-cycles:



Fig 4.13 Duty-cycles generation.

Figure 4.14 (A) shows how the PWM principle works. The orange trace is the triangle wave reference voltage, and the blue trace is the voltage from the pot. When the input voltage is greater than the reference voltage, the MOSFET turns on, and current flows in the load.



Fig 4.14 Output control signals.

The PWM signal is shown in blue figure 4.14(B),and finely the output PWM signals for the H-bridge inverter are shown in figure 4.14(C and D), the control signals are symmetrical the switch 1 with switch 4,and switch 2 with switch 3, this is for generating symmetrical output voltage .

After starting the simulation ,the output voltage of the power stage inverter is shown in Fig 4.15 as unfiltered output with switching effects. Its amplitude of peak voltage switched to

approximately between -325V and +325V through zero. When all the parameters in the inverter reach steady state, the output of the inverter will switch between positive to negative peak of the DC-link voltage, the output voltage without L-C-L filter is shown in the first part of the figure 4.15.

This voltage is then filtered by the L-C-L filter designed in this thesis to minimize these distortions. The clear output voltage is depicted in the second part in Fig. 4.15.



Fig 4.15 Inverter output voltage.

These results proved the performance of the stricter inverter chosen and also the type of control (unipolar PWM) .

4.1.2.2 Grid connected H-bridge inverter simulation

After the testing of the H-bridge inverter without electrical grid, and getting great results, now it is the time to test the performance and flexibility for this inverter with the connection of electrical grid.

The figure 4.16 shown the block simulation of H-bridge grid connected inverter with PV source, for making control the current and voltage of the output inverter, I_{grid} and V_{grid} are very necessary for it.



Fig 4.16 MATLAB Model of grid connected PV inverter.

Output waveforms of the grid connected PV inverter in figure 4.16 shows at the Matlab stable response of the grid voltage, this figure shown in the firstly part the H-bridge output voltage without filter and second part shown this voltage after uses the LCL filter, this filter it is interface between the H-bridge inverter and the grid, the grid voltage shown in the third part, the lastly part in this figure shown two voltage signals, the output voltage of the PV inverter and grid voltage, the phase between them is 0° for integrate the active power.



Fig 4.16 Output voltages : output voltage of H-bridge inverter ,the output voltage with LCL filter , grid voltage, superposition h-bridge inverter and grid voltages .

The grid connected H-bridge inverter simulation getting very well results, these results prove the performance of the grid control (PLL) and the design and values of the deferent output filter components.

4.2 Experimental results for Grid connected PV inverter

After making the simulation of the all PV Inverter parts and getting well results, now for validation this results the experimental testing is very important, this part shows the experimental testing for the PV inverter.

A prototype was built based on the inverter specification. The PV inverter controller is implemented fully on a 16bits fixed point *dsPIC30F4011 Microship* microcontroller.

Voltage and current signals are sampled using the internal 10-bit analog-to-digital converter inside the microcontroller. The output compare module of the microcontroller allows the modulation signal to be compared with an internal timer signal to resemble a PWM function block.

In the experimental setup, a DC voltage source which has a greater magnitude than the regulated DC-link voltage is connected at the DC-link capacitor through a variable resistor so that the DC-link gets roughly a constant current from the DC source. This is used to emulate the front end DC/DC converter in the PV system. The experimental card is shown in Figure 4.17. All schemas of sensors and the control and power card are shown in (appendix D).



Fig 4.17 Final experimental PV inverter card.

This card consisted on two principal parts, the first part is the flyback DC/DC converter included the control of maximum power point MPPT, the second part is the H-bridge inverter guaranteed the AC output voltage depended on the control grid current and voltage.

Firstly we will testing this card for control the maximum power point using the proposed variable step size incremental conductance IC MPPT, then we will also testing the all card directly from the input DC-PV voltage to electrical grid connected. All experimental results getting will disrupted and discussed in the next titles.

4.2.1 Experimental results of the proposed variable step size IC MPPT

To evaluate and verify the efficiency of the proposed variable step size and fixed step size ICMPPT methods, experiments have been carried out. Schematic of solar panel connections in the experiments PV system with the proposed MPPT controller is illustrated in Fig. 18.

Four solar panels connected in series MSX-60 are adopted as the PV array model in experiment tests, a prototype of the Flyback chopper converter and control circuit was implemented.



Fig 4.18 Schematic of solar panel connections in the experiments PV system with the proposed MPPT controller.

ThedsPIC30F4011 was used to provide the control signals for the Flyback converter, severall amps as load, two Hall-effect sensors LA100 and LV-25 have been used to detect the PV output current and the PV output voltage. The specifications are listed in Table4.2.

Solar panel	4 x MSX-60
The load Lamps	$100 \text{ W} \times 2$
The Flyback Chopper Inductance Capacitor Diode super fast Switch Digital controller	1 mH 440 μF U1640 (16A , 600 V) MOSFET IRFP460 (500 V, 20 A)
Controller Switching frequency	dsPIC30F4011 50 KHz

Table 4.2 Specifications experimental prototype.

Two experiments were performed on experimental prototypes that were designed, in which a comparison between the proposed variable step size IC MPPT method and the fixed step size IC MPPT method was presented; the duty cycle was initialled at zero for both methods. figure 4.19 shows the PV output current, the PV output voltage and PV output power

obtained by fixed step size IC MPPT methods corresponding to the 800W/m2, while figure 4.19 shows PV array output performance (PV output current and the PV output voltage and PV output power) with variable step size IC MPPT under constant irradiation (800W/m2).



Fig. 4.19. PV array output performance (PV output current and the PV output voltage and PV output power) with fixed step size IC MPPT under constant irradiation (800W/m2).



Fig. 4.20. PV array output performance(PV output current and the PV output voltage and PV output power) with variable step size IC MPPT under constant irradiation (800W/m2).

From Figs. 4.19 and 4.20, we can see that both the MPPT algorithms discussed in this paper have consider able accuracy. The power values given by the proposed variable step size and

fixed step size IC MPPT methods are very close to the theoretical value corresponding to the irradiation levels. We can clearly see that the response time of the proposed variable step IC algorithm is less than 0.5s, while it is about 3.7s in the fixed step IC method, even in steady state. This demonstrates that proposed method has a good tracking rapidity. The experimental results of the proposed MPPT algorithm present good accuracy, faster converging speed, less response time, no steady state oscillation around the MPP. Thus, the proposed variable step size IC MPPT algorithm is more suitable to practical operating conditions.

4.2.2 Experimental results of the PV inverter

After testing the control of MPPT and garneted the good results, now the lastly experimental testing is testing all parts in this card, this means testing the flyback converter with the H-bridge inverter connected in the electrical grid and PV source for the DC input.

The figure 4.21 shows the steady state operating DC-Link of the PV source, H-bridge inverter, output interface filter and the grid. In this configuration there are five main parts, the first is the control part consisted on the same microcontroller of the flyback *dsPic30F4011*, this controller making the management of the flyback converter and the H-bridge inverter based on parameters of voltages (V_{pv} , V_{dc} , V_{out} , V_{grid}) and currents (I_{pv} , I_{dc} , I_{grid}), the second part is the sensors, for getting the necessary parameters, the good sensing is very important, for this the high quality voltage and current sensors was used (LV-25 and LA-100 hell effect).

The third part is the Mosfets drivers, for driving the high side and low side gates the uses TLP250 is very clever choose, this ship is asserted the driving and the isolating power part in the same time .

In the fourth part the H-bridge inverter was shown, this consisted of two main arms based on four Mosfet's. 7N65 mosfets were model chosen as these devices have voltage and current parameters of 650 volts and 7 amps respectively. The final section consists of an output filter based on an LCL design from the parameters calculated in the chapter three.



Fig. 4.21. Schematic of grid connected solar inverter.

On completion of the construction of the solar inverter, voltage waveforms were monitored. These results are shown, firstly in figure 4. 22 which shows the Mosfet signals for S1 and S4 switches in the upper yellow trace and S2 and S3 switches in the lower blue trace. Here it can be seen that these signals are complementary. It should be noted that the dead time between the upper and lower drive signals is critical and essential for mosfets device security. It was determined that 0.5 ms was adequate for this protection, and this delay time is illustrate in figure 4. 23 below.



Fig. 4.22. Control switches signals .

As shown in Fig. 4.21 the microcontroller signals are applied directly to the mosfet drivers TLP250. These drivers then supply the control signals to establish high side and low side mosfets gate functions. As a result these control signals generated a PWM output signal with peak to peak voltage values of +325V to -325V. This inverter output is illustrated in the figure 4.23 below.



Fig. 4.23. Output voltage of the PV inverter.

As discussed earlier in order to obtain a sinusoidal output voltage a LCL filter was devised, the parameters were calculated as outlined in chapter three. The resulting filtered waveforms are illustrated in figure 4.24. To establish signal purity a FFT analyser was employed to measure harmonic distortion related to the 50Hz fundamental signal frequency. This indicted distortion levels of -13dB at 150 Hz , 1.48db at 250Hz , -25.3 db at 350 Hz and -4.8db at 450Hz .



Fig. 4.24.Output voltage with LCL filter and FFT analyser.

After obtaining optimal results using the LCL filter, the next crucial issue to be addressed is the voltage grid synchronisation. In order to accomplish this control was needed the of the grid voltage signals via a zero crossing circuit, this is explained and shown in (appendix D). The grid voltage and the PV inverter voltage are shown in figure 4.25 below, this illustrates the control grid efficiency. The oscilloscope trace shown in left indicates the starting time for the PV inverter whilst the right hand trace shows the associated output waveforms



Fig. 4.25. Synchronisation grid tasting.

The realised inverter exhibits large efficiency gains in all sections, the power section, the control section as well as the sensing section. This performance was verified by testing the final assembly in a variety of conditions.

Conclusion

This chapter has presented both simulated results and experimental verifications of the proposed inverter employing variable step size IC MPPT with flyback converter tecniques. These results confirm the novel approach and prove the proposed MPPT delivers high performance and flexibility for tracking the maximum power under the differing and variable climatic conditions. An H-bridge inverter was also simulated and developed to the prototype cardstage. As a result of these simulations and experimental results compatability between the various component parts of the grid connected PV inverter (Flyback and H-bridge)has been proven. These results in dicated a device that exhibits both versatility and high performance under challenging and variable operating conditions.

General conclusion and future researches

In this thesis, a grid connected PV inverter has been presented. The research in this context is divided into two main sections: the first section the flyback DC/DC converter with the control of MPPT and the second section is the H-bridge inverter with the grid connection control. Additionally, the overall system design and implementation have been discussed in details.

A new modified variable step size Incremental Conductance MPPT algorithm with direct control has been proposed. A comparative study between the proposed variable step size and fixed step size Incremental Conductance MPPT method under similar operating conditions has been addressed. The simulation results demonstrate huge contributions on the steady state performance and the dynamic response. A significant improvement in the maximum power point tracking, time response using variable step size Incremental Conductance MPPT has been validated and thus additionally the energy loss is reduced. The improvement of variable step size IC MPPT method with respect to ripple and overshoot are clearly observable. The experimental results of the proposed MPPT algorithm show an excellent accuracy, faster converging speed, less oscillation around the MPP, and no divergence from the MPP point. Therefore, the proposed variable step size Incremental Conductance MPPT algorithm is efficient and more likely to be associated with better noise rejection and less energy loss.

Unipolar PWM, control of the voltage and current and the synchronisation (PLL) have been implemented for the H-bridge inverter, and also the DC-link between the flyback converter and the H-bridge inverter has been controlled.

The controllers included in the microcontroller (dspic30F4011) and the sensors are designed in this thesis, which includes: a Maximum Power Point Tracker (MPPT) for optimizing the captured energy from the PV module, a Phase Locked Loop (PLL) to synchronize the inverter with the grid, detection of islanding operation, control of the DC-link voltage, and control of the grid current.

Finally, the theoretical investigation and simulation approach of the grid connected PV inverter have been further validated by experimental studies.

Proposals for future works are summarized:

- ➢ In the Grid Connected PV system, there is a great need of designing the control system that could control the designed inverter power for the smart grid. The control would ensure the integrating the inverter with other renewable energy sources available.
- Analyze and optimisation the impact of this inverter on the grid performance or the power quality.
- And finally, the next step for product development is to optimize the inverter in respect to the microcontroller, the switch mode power supply, measuring and protection circuits, etc.

Appendix A

h ma	0.2	0.4	0.6	0.8	1.0
Fundamental	0.2	0.4	0.6	0.8	1.0
m_{f}	1.242	1.15	1.006	0.818	0.601
$m_f \pm 2$	0.016	0.0061	0.131	0.220	0.318
$m_f \pm 4$					0.018
$2m_f \pm 1$	0.190	0.326	0.370	0.341	0.181
$2m_f \pm 3$		0.024	0.071	0.139	0.212
$2m_f \pm 5$				0.013	0.033
$3m_f$	0.335	0.123	0.083	0.171	0.113
$3m_f \pm 1$	0.044	0.139	0.203	0.176	0.062
$3m_f \pm 3$		0.012	0.047	0.104	0.157
$3m_f \pm 5$				0.016	0.044
$4m_f \pm 1$	0.163	0.157	0.008	0.105	0.068
$4m_f\pm 3$	0.012	0.070	0.132	0.115	0.009
$4m_f \pm 5$			0.034	0.084	0.119
$4m_f \pm 7$				0.017	0.050

Harmonics Table for Switch Mode Inverters

Table A.1: Generalized harmonics of V_{Ao} for a large m_f

Appendix B

Cercuit PCB of the PV inverter



Fig B.1 PCB board of the PV inverter



Fig B.2 3D PCB for PV inverter

Appendix C

Datasheets of the PV inverter Components

1/ Microcontroller dsPic30F4011



Fig B.3 dspic30F4011

High Performance Modified RISC CPU:

• Modified Harvard architecture

- C compiler optimized instruction set architecture
- with flexible addressing modes
- 84 base instructions
- 24-bit wide instructions, 16-bit wide data path
- 48 Kbytes on-chip Flash program space
- (16K Instruction words)
- 2 Kbytes of on-chip data RAM
- 1 Kbytes of non-volatile data EEPROM
- Up to 30 MIPs operation:
- DC to 40 MHz external clock input
- 4 MHz-10 MHz oscillator input with
- PLL active (4x, 8x, 16x)
- 30 interrupt sources
- 3 external interrupt sources
- 8 user selectable priority levels for each
- interrupt source
- 4 processor trap sources
- 16 x 16-bit working register array
- DSP Engine Features:
- Dual data fetch
- Accumulator write back for DSP operations
- Modulo and Bit-Reversed Addressing modes
 Two, 40-bit wide accumulators with optional
- saturation logic
- 17-bit x 17-bit single cycle hardware fractional/ integer multiplier
- All DSP instructions single cycle
- \pm 16-bit single cycle shift
- Peripheral Features:
- High current sink/source I/O pins: 25 mA/25 mA

Motor Control PWM Module Features:

- 6 PWM output channels
- Complementary or Independent Output
- modes
- Edge and Center Aligned modes
- 3 duty cycle generators
- Dedicated time base
- Programmable output polarity
- Dead-time control for Complementary mode
- Manual output control
- Trigger for A/D conversions
- Quadrature Encoder Interface Module
- Features:
- Phase A, Phase B and Index Pulse input
- 16-bit up/down position counter
- Count direction status
- Position Measurement (x2 and x4) mode
- Programmable digital noise filters on inputs
- Alternate 16-bit Timer/Counter mode
- Interrupt on position counter rollover/underflow
- Analog Features:
- 10-bit Analog-to-Digital Converter (A/D) with
- 4 S/H Inputs:
- 500 Ksps conversion rate
- 9 input channels
- Conversion available during Sleep and Idle
 Programmable Brown-out Detection and Reset generation
- Special Microcontroller Features:
- Enhanced Flash program memory:
- 10,000 erase/write cycle (min.) for

- Timer module with programmable prescaler:
- Five 16-bit timers/counters; optionally pair
- 16-bit timers into 32-bit timer modules
- 16-bit Capture input functions
- 16-bit Compare/PWM output functions
- 3-wire SPITM modules (supports 4 Frame modes)
- I2CTM module supports Multi-Master/Slave mode and 7-bit/10-bit addressing
- 2 UART modules with FIFO Buffers
- 1 CAN modules, 2.0B compliant

industrial temperature range, 100K (typical) • Data EEPROM memory:

- 100,000 erase/write cycle (min.) for
- industrial temperature range, 1M (typical)
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT)
- and Oscillator Start-up Timer (OST)

• Flexible Watchdog Timer (WDT) with on-chip low power RC oscillator for reliable operation

• Fail-Safe clock monitor operation detects clock failure and switches to on-chip low power RC oscillator

- Programmable code protection
- In-Circuit Serial ProgrammingTM (ICSPTM)
- Selectable Power Management modes
- Sleep, Idle and Alternate Clock modes
- CMOS Technology:
- Low power, high speed Flash technology
- Wide operating voltage range (2.5V to 5.5V)
- Industrial and Extended temperature ranges
- Low power consumption

2/ Mosfet IRFP460



Fig B.4 IRFP460

- TYPICAL RDS(on) = 0.22W
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

DESCRIPTION

The PowerMESHTMII is the evolution of the first generation of MESH OVERLAYTM. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns swithing speed, gate charge and ruggedness.

APPLICATIONS

- SWITH MODE LOW POWER SUPPLIES (SMPS)
- HIGH CURRENT, HIGH SPEED SWITCHING
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVES

Table B .1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VDS	Drain-source Voltage (V _{GS} = 0)	500	V
VDGR	Drain-gate Voltage (R _{GS} = 20 kΩ)	500	V
V _{GS}	Gate- source Voltage	±30	V
ID	Drain Current (continuos) at T _C = 25°C	18.4	Α
ID	Drain Current (continuos) at T _C = 100°C	11.6	Α
I _{DM} (●)	Drain Current (pulsed)	73.6	Α
Ртот	Total Dissipation at T _C = 25°C	220	W
	Derating Factor	1.75	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
Тј	Max. Operating Junction Temperature	150	°C

3/ Driver Mosfet TLP250



Fig B.5 TLP250

Transistor Inverter

Inverter For Air Conditioner

IGBT Gate Drive

Power MOS FET Gate Drive

The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.

This unit is 8-lead DIP package.

TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: IF=5mA(max.)
- Supply current (ICC): 11mA(max.)
- Supply voltage (VCC): 10–35V
- Output current (IO): ±1.5A (max.)
- Switching time (tpLH/tpHL): 0.5µs(max.)
- Isolation voltage: 2500Vrms(min.)
- UL recognized: UL1577, file No.E67349
- Option(D4)
- VDE Approved : DIN EN60747-5-2

Maximum Operating Insulation Voltage : 890VPK

Highest Permissible Over Voltage : 4000VPK
4/ Diode MUR1640



Fig B.6 Mur 1640

MUR1640 ULTRAFAST PLASTIC RECTIFIER

Applications:

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Features:

- Ultra-Fast Switching
- High Current Capability
- Low Reverse Leakage Current
- High Surge Current Capability
- Plastic Material has UL Flammability Classification 94V-O
- This is a Pb Free Device
- All SMC parts are traceable to the wafer lot
- Additional testing can be offered upon request

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ملخص

اليوم، الحاجة للحصول على الطاقة يزيد باستمرار، وتصبح واحدة من أكبر التحديات التي تواجه العلماء والحكومات. ولذلك، فإن تطوير الطاقة المتجددة أصبحت ذات أهمية متزايدة. و من بين الحلول الطاقة المتجددة، والنظم الضوئية هي واحدة من مصادر الطاقة الواعدة. ومع ذلك، فإنه لديها بعض العيوب مثل انخفاض الطاقة المحصلة وغير خطية و التي تقدم نقطة واحدة لاستخراج الطاقة القصوى في هذا السياق، هدفنا في هذه الأطروحة هو تطوير وتحسين النظم الكهربائية الضوئية، حيث تم التحقق من صحة تصميم تحويل فلايباك جسر العاكس H متصل بالشبكة الكهربائية باستخدام SIMULINK وتم تطوير النموذج التجريبي. وبالإضافة إلى ذلك، تم تطوير خوارزمية جديدة TC MPPT باستخدام خطوة متغيرة واختبار ها بنجاح على نظام الضوئية على أساس تحويل فلايباك ودائرة التحكم .siguit التنائج العديد من التحقق.

الكلمات المفتاحية – العاكس المتصل بالشبكة الكهربائية الخاص بالأنظمة الكهروضوئية ، المحول فلايباك ، العاكس جسر (H-bridge) ، MPPT ، الشبكة الذكية ، المتحكم الصغير .

Résumé

Aujourd'hui, le besoin d'énergie augmente de façon continue et devient l'un des plus grands défis des scientifiques et des gouvernements. Par conséquent, le développement des énergies renouvelables devient de plus en plus très important. Parmi les solutions d'énergie renouvelable, le système photovoltaïque est l'une des sources d'énergie les plus prometteuses. Cependant, il est présente certains inconvénients tels que : faible rendement et la caractéristique P-V qui présente un point unique d'extraction de la puissance maximale (MPP). Dans ce contexte, notre thèse traite le développement et l'amélioration des systèmes photovoltaïques, dans lequel la conception du convertisseur Flyback, onduleur en pont H connecté au réseau ont été validées en utilisant Matlab / Simulink et le prototype expérimental développé. En outre, un nouvel algorithme IC MPPT utilisant un pas variable a été développé et testé avec succès sur un système photovoltaïque basé sur le convertisseur Flyback et un circuit de commande dsPIC30F4011. Les résultats obtenus démontrent de nombreuses contributions.

Mots clés – Système PV connecte aux réseaux, flyback, H-bridge ondeleur, MPPT, microcontrôleur dspic30F4011.

Abstract

With the current ever increasing demands for energy from conventional sources reaching critical levels and limitations on supply and demand, defying the best efforts of both scientists and governments to implement, the development of renewable energy sources is becoming increasingly important and viable. Among these renewable energy solutions, the photovoltaic system is one of the most promising energy sources. Such system show ever still present some significant drawbacks such as low efficiency and nonlinear P–V characteristics. This work addresses these issues using a number of novel techniques. In this context, our thesis deals the development and improvement of PV systems, in which design of Flyback converter, grid connected H-bridge inverter have been validated using Matlab/Simulink and developed experimental prototype. In addition, a new variable step-size incremental Conductance IC MPPT (maximum power point tracking) algorithm has been developed and tested successfully on a photovoltaic system based on Flyback converter and control circuit using dsPIC30F4011.The resulting techniques and development represents significant advances in the field of PV generation and control.

Keywords- grid connected PV inverter, flyback converter, H-bridge inverter, MPPT, smart grid, microcontroller dspic30F4011.