République Algérienne Démocratique et Populaire
Ministère de l'Enseignement Supérieur et de la Recherche Scientifique

Ecole Nationale Polytechnique

Département d'électronique
Laboratoire des dispositifs de Communication
et de conversion Photovoltaïque

Doctoral thesis in science

Option: Electronic Engineering

Study and wide band characterization of nanometric materials on SOI

Yasmina ATROUCHE-BELAROUSSI

Presented and publicly supported on 15/05/2018

Composition of the Jury:

President :	Mr. Cherif Larbes,	Professor	ENP
Advisor:	Mr. Mohamed Trabelsi,	Professor	ENP
Advisor:	Mr. Mohand Tahar Belaroussi,	Research Director	DGRSDT
Examiners :	Mr. Arab Azrar,	Professor	UMBB
	Mr. Mourad Adnane,	Senior Lecturer A	ENP
	Mr. Mouloud Challal,	Senior Lecturer A	UMBB
	Mr. Noureddine Gabouze,	Research Director	CRTSE
Invited member:	Mr. Jean-Pierre Raskin	Professor	UCL

ENP 2018

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ملخص

أدخلت هذه الأطروحة متغيرات جديدة من ركائز السليكون المسامية(PSi). بفضل قياسات الأداء التردد الراديو (RF). الركائز PSi المقترحة تمت مقارنتها للعديد من ركائز تستند على السليكون الصلب، من بينها، السليكون القياسي(dtS)، السليكون الغني بالفخاخ (TR) والسليكون عالي المقاومية (HR). وقد تم إدماج خطوط (CPW) على كل الركائز المذكورة ودراسة خصائصها إلى غاية الترددات الميليمترية (70جيجا هرتس). وأظهرت الركائز الجديدة (PSi) انخفاضا في السماحية النسبية الفعالة للركيزة إلى قيم منخفضة تصل إلى 3.7 وزيادة كبيرة في المقاومية الفعالة إلى قيم أكبر من 7 كيلو أوم سم. ومن أجل إظهار فائدة الركيزة (PSi) لتصميم دوائر التردد الراديو(RF) العاملة في نطاق المليمتر، تم دمج مرشاح ممر الموجة (MBPF) المركز عند 27جيجا هرتس على الركائز المدروس. بالمقارنة مع (MBPF) التقليدية التي تنفذ على ركائز القياسية على أساس السليكون الصلبة، وقد أظهرت معايير قياس S من (MBPF) على أساس (PSi) أداء الترشيح عالية، مثل الحد من خسائر الإدراج، وتحسين في الانتقائية للمرشح وكذلك زيادة في عامل الجودة، بالإضافة إلى ذلك، تم الحفاظ على هذا الأداء حتى مع تغير في درجة الحرارة، وقد أثبتت بشكل جيد فعالية ركائز (PSi) المقترحة.

الكلمات الدالة: مرشاح ممر الموجة (FBP)، ارتفاع في درجة الحرارة، موجة ملليمتر، الحد الأدنى فقدان الإدراج، السليكون المسامية (PSi).

Résumé : **Etude et caractérisation large bande de matériaux nanométriques sur SOI**

Dans cette thèse, de nouvelles variantes de substrats en silicium poreux (PSi) ont été introduites. Grâce aux mesures des performances RF, les substrats PSi proposés ont été comparés à différents substrats à base de silicium massif, à savoir, le silicium standard (Std), le silicium riche en piège (trap-rich) (TR) et le silicium à haute résistivité (HR). Des lignes CPW ont été intégrées sur tous les substrats mentionnés et une caractérisation jusqu'aux fréquences millimétriques (70 GHz) a été effectuée. Les nouveaux substrats PSi ont montré une réduction de la permittivité relative effective du substrat à des valeurs aussi basse que 3,7 et une augmentation considérable de la résistivité effective à des valeurs supérieures à 7 kΩ cm. Afin de démontrer l'utilité du substrat PSi pour la conception des circuits RF fonctionnant en bande millimétrique, un filtre passe-bande (MBPF) centré à 27 GHz a été intégré sur les substrats étudiés. Par rapport au MBPF classique mis en œuvre sur des substrats standards à base de silicium massif, les paramètres S mesurés du MBPF à base de PSi ont montré des performances de filtrage élevées, comme la réduction des pertes d'insertion, une amélioration de la sélectivité du filtre ainsi qu'une augmentation du facteur de qualité, de plus, ces performances ont été maintenue même avec le changement de la température, l'efficacité des substrats PSi proposés a été bien mise en évidence.

Mots-clés : Filtre passe-bande (BPF), Haute température, Onde millimétrique, Perte d'insertion minimale, Silicium poreux (PSi).

Abstract

In this thesis, new variants of porous silicon (PSi) substrates have been introduced. Through RF performance measurements, the proposed PSi substrates have been compared with different silicon-based substrates, namely, standard silicon (Std), trap-rich (TR) and high resistivity (HR). All of the mentioned substrates have been fabricated where identical samples of CPW lines have been integrated on and characterization to the millimeter wave frequencies (70 GHz) was performed. The new PSi substrates have shown successful reduction in the substrate's effective relative permittivity to values as low as 3.5 and great increase in the effective resistivity to values higher than 7 kΩ.cm. As a concept proof, a millimeter-wave bandpass filter (MBPF) centered at 27 GHz has been integrated on the investigated substrates. Compared with the conventional MBPF implemented on standard silicon-based substrates, the measured S-parameters of the PSi-based MBPF have shown high filtering performance, such as, a reduction in insertion loss and an enhancement of the filter selectivity. Having obtained the same filter performance by varying the temperature, the efficiency of the proposed PSi substrates has been well highlighted.

Keywords: Bandpass filter (BPF), High temperature, Millimeter-wave, Minimum insertion loss, Porous silicon (PSi)

"The art of being sometimes very daring and sometimes very careful is the art of succeeding "

Napoléon Bonaparte

Acknowledgments

بسم الله الرحمان الرحيم

In the Name of God, the Most Gracious, the Most Merciful

All praise is due to ALLAH, the almighty, for giving me the strength and power to start and finish this work.

First of all, I would like to thank my PhD supervisors: Prof. Mohamed Trabelsi, and Dr. Mohand Tahar Belaroussi for the follow-up of my thesis, their patience, and the trust they have granted on me throughout these years.

I wish to thank all the jury members, who have kindly accepted to be part of my thesis Jury and for the honor they granted me by agreeing to examine my work and particularly Prof. Cherif Larbes for having agreed to chair this Jury.

I would like to express my heartfelt gratitude to Prof. Jean-Pierre Raskin for having hosted me in the ICTEAM laboratory at the Université Catholique de Louvain, Belgium for eighteen months, during which I had the immense privilege and the honor to interact with him and the other members of his group. I would also like to thanks him for his sympathy, support and valuable advices. I do not forget to express my gratitude and thankfulness to Pascal Simon, the technical manager of the WELCOME platform. I am grateful to ICTEAM administrative and technical staffs for their help, and all the WINFAB clean-room team Christian, Andre, Miloud and Ester. My special thanks also go to all friends whom I met during this PhD journey, Gilles, Khaled, Martin, Mostafa, Jonathan, Laurent and Mohamed. Last and the best important, special thanks go to all my friends, who adopted me and being my second family during my stay in Belgium for your support, friendship, care and love: Lila, Kinda, Assia, Lamia, Donia, Karima, Nora, Ibtissem, Siham, and Dina.

I would like to thank Dr. N. Gabouze for opening the doors of the CMSI (Thin Films, Surfaces and Interfaces) laboratory of CRTSE and the interest carried for my work.

A lively thanks for my colleague Dr. Ahmed Abdelhalim Saadi for all his scientific discussions, his advice, his precious reading, correction of the memory, and especially for his moral support. My thanks for my dear friends Karima and Amel.

I thank my husband who always encouraged me to go ahead. A warm thanks for my mother and mother in law for their prayers.

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Acronyms

AFM	Atomic Force Microscopy
BOX	Buried Oxide
BPF	Band Pass Filter
CMOS	Complementary Metal-Oxide Semiconductor
CPS	Coplanar Striplines
CPW	Coplanar Waveguide
DUT	Device Under Test
EDS	Energy Dispersive Spectroscopy
FTIR	Fourier Transform Infrared Spectroscopy
PVD	Physical Vapor Deposition
HD	Harmonic Distortion
HF	hydrofluoric acid
HR-Si	High Resistivity Silicon
HR-SOI	High Resistivity SOI
IoT	Internet of Thing
KOH	Potassium Hydroxide
MNFM	Metallic-nanowire-filled-membrane
mm-wave	millimeter-wave
MOS	Metal-Oxide-Semiconductor
MS	Micro Strip
PECVD	Plasma-Enhanced Chemical Vapor Deposition
pMOS	Metal-Oxide-Semiconductor with p-type silicon substrate

PSC	Parasitic Surface Conduction
PSi	Porous Silicon
PSi-M	Porous Silicon from a nominal resistivity p-type Si wafer (5-20 mΩcm)
PSi-S	Porous Silicon from a standard resistivity p-type Si wafer (1-10 Ωcm)
RF	Radio Frequency
RMS	Root Mean Square
S-CPW	Slow-Wave Coplanar Waveguide
SEM	Scanning Electron Microscope
SiO_2	silicon oxide
SN	Sensing Nodes
SoC	System-on-Chip
SOI	Silicon-On-Insulator
SOLT	Short-Open-Load-Thru
Std	Standard
SW-μstrip	Slow wave μicrostrip
TL	Transmission Lines
TMH	TetramethylammoniumHydroxide
TRL	Thru-Reflection-Load
TR	Trap-Rich
TR-Si	Trap-Rich Silicon
VNA	Vector Network Analyzer
WPAN	Wireless Personal Area Network
XRD	X-Ray Diffraction

List of symbols

$At\%$	Atomic percentage
α	Attenuation coefficient
Z_C	Characteristic impedance
ξ	Correlation length
ρ_{eff}	Effective resistivity
H	Hardness
ρ	Nominal resistivity
ε	Permittivity
γ_{Si}	Poisson's ratio
P	Porosity
P	Power spectral density
Q	Quality factor
ε_{reff}	Relative effective permittivity
σ (r)	RMS roughness
σ	Stress
t_{PSi}	Thickness of porous silicon film
t_{Si}	Thickness of silicon
ε_0	Vacuum permittivity
E	Young’s modulus
E_{Si}	Young's Modulus of silicon substrate
$Wt\ \%$	Weight percentage

W	Signal line Width
S	Signal-to-ground line distance
W_g	Ground-line-width
f_e	Dielectric relaxation frequency

General Introduction

GENERAL INTRODUCTION

At the dawn of 2020 the deployment of Internet of Thing (*IoT)* will become a reality. The concretization of IoTis unsurprisingly based on the concept of sensing network in which the sensing nodes (SN) will attract major interest towards the success of this challenge. A massive production of these SNs will emerge, and industrials will need to tradeoff between efficiency and cost to keep the competiveness of their products. In fact, to accomplish this tradeoff, a suitable choice of the components should be performed, the use of emergent active devices is highly recommended **[1],** and the quality factor of passive components should be accounted for **[2].** One of the most important aspects impacting the performance of these components is the good choice of the substrate on which the SN is integrated. Indeed, bulk silicon is the most widely used substrate for the integrated circuits in the semiconductor industry. However, due to its high electrical conductivity and high-frequency losses, bulk silicon substrate suffers from significant losses at high frequencies which drastically reduce the RF performance of passive and active devices **[2].** This degradation becomes more severe at millimeter-wave (mm-wave) frequencies.

In addition, the growing trend in mm-wave design is to go toward realizing fully integrated Front-end. Therefore, the integration of both passive and active analog circuits on the same chip with the digital part becomes inescapable. High isolation between different circuits lying on the same substrate should be considered, thus, the cross-talk must be reduced. Thus, substrates with high resistivity and low permittivity should be utilized.

By observing the current trends of microelectronics industry we can note the convergence toward the integration of RF circuit on SOI (Silicon on Insulator) especially with the introduction of trap-rich substrates. Indeed, ICTEAM laboratory at UCL in Belgium has proved an expertise in this area since they have proposed trap-rich substrate, which has been already adopted by industrials, for instance, SOITEC. Nonetheless, it is pertinent to report the care of the scientific community about the suitability of trap-rich for the integration of mm-wave circuits.

For the above reasons, and to continue on the same scope, we tried over the current work to replace the trap-rich substrate by the porous silicon substrate. We believe that the porous silicon is adve rtised as the good candidate thanks to its low cost and short process and it constitutes suitable alternative to trap-rich.

Various Si-based substrates, compatible with Silicon-on-Insulator (SOI) CMOS process, have been proposed to overcome the problem of performance degradation such as High Resistivity SOI (HR-SOI), Trap-Rich Silicon (TR-Si)**[3−7]** as well as nanocrystalline porous silicon which is a very promising alternative to bulk silicon substrates for the fabrication of low cost RF circuits **[8].** Porous Si exhibits low permittivity, whose value depends on the porosity between those of air ($\varepsilon_r = 1$) and that of silicon ($\varepsilon_r = 11.7$) **[9].** It can be fabricated from aSi wafer by electrochemical dissolution of bulk crystalline silicon. The main advantages of PSi are, its very low cost, and its CMOS process compatibility enabling the integration of both passive and active devices on the same substrate, and thus the development of a System-on-Chip (SoC). Furthermore, most investigated porous silicon substrates for RF applications are mesoporous made from n-type **[9]** and p+-type doped silicon owning a nominal resistivity lower than 20 mΩcm **[8−14].** In fact, many PSi-based materials were found suitable for a wide range of integrated circuits with high performance, as it has been demonstrated in previous studies **[15 − 18].**

Actually, the integration of mm-wave circuits in porous silicon has been already investigated through various works, as we can see over the references cited in this thesis. However, the research on this topic remains and the researchers continue to enhance the quality of the proposed porous silicon. In this context, we aimed to propose improved porous silicon substrate compared with those presented in the literature.

The foreseen objective is to optimize all parameters, in order to present high quality porous silicon substrate especially when mm-wave applications are accounted for. By considering these applications, the proposed porous silicon should own pores size less than 5 nm**[19]**, anodized layers with high uniformity and sufficiently spongy structure, all of these, to reach high insulating properties and low permittivity thus high quality factor (see Table 1).

Substrate	Bulk thickness (μm)	Nominal resistivity (Ωcm)	Porous thickness (μm)	Porosity and pore diameter	Oxide thickness (nm)	α (dB/mm)	Q@26/60GHz	Fabrication cost estimation
Std	381± 20	1 - 10	---	---	500	3.8	2.1/4.9	High
HR	725 ± 25	> 4k	---	---	500	1.6	4.5/10.5	High
TR	725 ± 25	> 10k	---	---	500	0.35	20.6/47.5	High
PSi-S	381± 20	1 - 10	50	65% < 5 nm	500	0.18	25.2/58.3	Low
PSi-M	381± 20	5 - 20 m	50	50% ~ 12 nm	500	0.34	16.0/36.9	Low

Table 1. Substrates characteristics

Finally, the reached characteristics besides the low cost make the proposed porous silicon original compared with those already published in previous work. Moreover, to emphasize the high quality of the realized substrate, as concept proof, mm-wave filters have been integrated on, while they are usually based on 0.18-μm and 0.13-μm CMOS technologies. As we have observed over the presented results, a successful reduction in insertion loss has been achieved. Also, to the best of author knowledge, this is the first mm-wave bandpass filter integrated in PSi substrate.

Consequently, to summarize the originality of our work four main aspects should be considered. First, the low cost development compared with generally used process for the integration of mm-wave circuits. Second, the low complexity process. Third, the new variant of porous silicon having high insulating properties and high quality factor as depicted in Table 1. Forth, the performed high temperature analysis showed the reliability of the proposed PSi.

The scope of this work isto investigate RF performances of the Si-based substrates (Std, HR, TR and PSi) and their suitability to co-integrate on-chip passive elements and active devices for RF and system-on-chip applications.

This thesis is organized as follows:

1. Chapter 1, brings together the substrates technologies for RF applications, and introduces porous silicon as substrate with some of his applications area. In this thesis five types of Si-based substrates are compared.
2. Chapter 2is dedicated to elaboration and physical characterization of porous silicon PSi for RF application
3. In chapter 3, we present the integration of CPW lines on PSi substrate using a low complexity fabrication process (see Annex A), with their wide band characterization, and we have observed their behavior at high temperature up to 175°C after their submission to temperature variation and compared with their respective counterpart TR, HR and Std substrates.
4. In chapter 4, we propose a demonstrator on Si based substrates, a bandpass filter is designed around the frequency of 27 GHz and fabricated on top of Std, HR, TR and PSi substrates. A good agreement between simulations and measurements results is obtained. We have compared the performance of the PSi-based mm-wave filter to relevant works tied to mm-wave filters fabricated in various CMOS technologies.in this context, we have submitted the filter to temperature variation up to 175°C, the filter response remains almost unchanged even at high temperature.
5. A general conclusion of this thesis is presented in chapter 5 that highlight the efficiency of PSi substrate. Therefore, the proposed porous silicon substrate offers low cost alternative to 0.18-mm CMOS technology and trap rich technology, especially when mm-wave circuit design is accounted for.

Chapter 1

SUBSTRATES TECHNOLOGIES FOR RF APPLICATIONS

1.1 Introduction

In the fields of microelectronics, photonics, optoelectronics, radiofrequency (RF) applications or high power devices, the selection of the appropriate semiconductor substrate technology is a critical issue. Indeed, suitable selection can provide a capital advantage to achieve high performance. RF and microwave systems, require specific back-end-of-line to fulfill their needs, substrates such as standard silicon or high resistivity (HR) silicon have been widely used. However, the increasing expansion of RF applications, such as 5G telecommunication, high data rate WPAN (Wireless Personal area Network), and *IoT* (Internet of things), leads to new requirements for the integration of digital and analog devices on the same chip like, low loss, low cost and manufacturing easiness; these constraints become more important especially when frequencies higher than 20 GHz are targeted.

Thus, before going toward the treated topic by this thesis, it is appropriate to review the commonly used substrates in the industry of microelectronics.

1.2 Description of substrates for RF applications

1.2.1 Standard silicon substrate (Std)

From a physical and mechanical point of view, a classical solid substrate is made up of silicon, the maturity of silicon technologies and the progress of MOS transistors in the microwave domain, explains the success of silicon compared to III-V technologies **[20-23]**.

Since the 80s, CMOS technology has become the dominant technology for integrated circuits. The manufacture of RF components involves the use of substrates favoring weak

energy losses. These losses are of two types. Capacitive losses by coupling with substrate and eddy current losses induced in the substrate.

1.2.2 High Resistivity Silicon-on-Insulator substrate (HR-SOI)

RF SOI is composed of a top layer a thin film of monocrystalline silicon, an isolation layer as an oxide and a high resistive substrate as the handle substrate. Although, High-resistivity substrates (HR-Si, HR-SOI) (Fig 1.1) are compatible with the processes and manufacturing CMOS circuits **[24-25]**, they still suffer from crosstalk and parasitic surface charges (PSC). In the RF SOI products, the oxide of the insulator BOX still contains positive charges, those charges create a parasitic surface conduction at the interface between the BOX and the high-resistivity handle substrate **[7,26]**. A new substrate that do not suffer as much from the parasitic effects and crosstalk is the ideal for RF applications, one could think of about a glass or quartz substrates. However, their high thermal resistance can lead to self-heating phenomena **[27]**, we are going to discover this new substrate in the next section.

Figure 1.1 High Resistivity wafer

1.2.3 Trap-rich high resistivity substrate TR-Si

The proposed substrate resistivity can reach several kΩ.cm. This high-resistivity characteristic, translates to very low RF insertion loss along coplanar waveguide (CPW) transmission lines and purely capacitive crosstalk similar to quartz substrate **[28]**. This means get around the parasitic effect and crosstalk.

J-P. Raskin and coworkers **[29-31]** have invented a technic consisting of adding a rich trap-rich poly silicon layer underneath the buried oxide as shown in Figure 1.2, it is the best

method for reducing the surface parasitic effect (PSC) which degrades the high resistivity properties of HR-Si substrates, thus increasing their losses **[32].**

Figure 1.2 Trap-rich wafer

1.2.4 Porous silicon substrate PSi

A new promising substrate that could be the solution to the integration problem may be the porous silicon (PSi). As discussed in **[33]**, this material can be locally formed on the Si plate by electrochemical dissolution of solid crystalline Si **[34]**. Figure 1.3 represent the porous silicon substrate PSi with an SiO_2 layer.

Figure 1.3 Porous Silicon wafer

The properties of PSi are highly dependent and can be driven by the electrochemical conditions used during anodization. For RF circuits, the desirable characteristics are low dielectric constant and low loss, which will be explained later in this thesis.

The high permittivity of the bulk Si increases the crosstalk between the lines, decreases the antenna efficiency and the maximum operating frequency in the inductors. This could lead to the conclusion that PSi should have as high a porosity as possible to approach air permittivity (ε_r= 1), but the situation is not so simple since the increase of porosity, increases fragility substrate.

Different morphologies lead to different degrees of interconnection in the substrate. More oriented structures leave an electric path for the eddy currents, leading to the higher

polarization loss. However, the random distribution of pores in moderately propagated structures has shown promising results due to the reduction of eddy currents in the substrate **[35]**. Another factor that has an impact on the parameters of interest is the annealing step. During annealing, the thin layer of oxide on the walls of the pores grows in a controlled manner. The PSi may be fully oxidized, the oxide has fixed charges, which can polarize the surface and create a highly conductive layer all along the boundary of the pores that are the walls of bulk silicon.

In view of all the above, it is essential to carefully select the morphology of the porous silicon layer PSi so as to optimize the RF parameters if the PSi is to be used as an RF substrate.

1.3 The Physics of porous silicon

1.3.1 Introduction

Porous silicon is a well-known material produced by anodization of silicon in hydrofluoric acid (HF)-based electrolyte. A number of factors determine the pore morphology. Though each of types of pores (micro, meso, and macrospores) has been extensively investigated and can be produced under a variety of conditions **[35-37]**. Other technological solutions have also been proposed using silicon nano-pillar arrays to create a vertically oriented field effect transistor for the decoupling of device density from channel length **[38-40]**.

The ability to insert a thick porous silicon layer on a low resistivity Si wafer, on which the RF devices can be integrated, enabled the elaboration of insulating/semiconductor mixed substrates **[8-41]**. In fact, this material exhibits low permittivity, whose value depends on the porosity between those of air (ε_r = 1) and silicon (ε_r = 11.7) **[9]**. Moreover, most porous silicon substrates studied in the literature for RF applications are mesoporous and made from p-type silicon of resistivity below 10mΩ.cm. The materials are generally of moderate thicknesses (10 to 200µm) with porosities of 70 to 80% **[42-44]**. Furthermore, porous silicon on n-type substrates in the field of radio frequencies has also been demonstrated in terms of electrical insulation while maintaining low mechanical stresses in the substrate and good thermal conduction **[10]**.

Additionally, the ease and low cost of obtaining porous Si and its particular electrical, optical and thermal properties make this material a field of development for microsystems. In this context, it appears possible to combine the use of several of these properties in a single integrated micro device. As of the use of its dielectric properties, porous silicon implementation has been most often made in the form of thick insulating boxes mainly in the field of radio frequencies **[45-46]**.

1.3.2 History of porous silicon PSi

Porous silicon (PSi) is a structural form of silicon chemical element. It has a large surface to volume ratio due to a large number of micro-, meso- and macropores. In most PSisamples, these pores are mainly oriented in the crystallographic direction **[47]**, and are carried out in the platelet by electrochemical dissolution, mainly using aqueous or ethanoic solutions of hydrofluoric acid (HF) .

The first realization of a layer of porous silicon was made by A. Uhlir in 1956 **[48]** during his work on electropolishing. This discovery initially aroused interest in the production of SOI (Silicon On Insulator) substrate by increasing the dielectric property of the porous by its oxidation **[49-50]**. The following was L.T.Canham's by discovering the high luminescence of porous silicon at ambient temperature**[51]**, that this material was devoted with high interest and became the main research object **[52-55],** during coming years. Nonetheless, PSi continues its investigation and new ideas are explored, from biosensors to RF applications.

1.3.3 Nanostructuring and morphology

The porous silicon has a nanostructured form of monocrystalline silicon, its degree of anodization is defined by the rate of layer formation and porosity, with the pore morphology which depends on the type of wafer and the resistivity, the applied current density as well as process duration, and the composition of the electrolyte (HF concentration, with or without additives). Its morphology is usually classified into three categories according to the diameter of the silicon nanocrystallites that make it up. Their size can range from a few nanometers to a few micrometers, so we will speak of silicon **[56]**:

- micro-porous: crystallites between 1 and 5 nm
- meso-porous: crystallites between 5 and 50 nm

• macro-porous: crystallites greater than 50 nm

For all the morphologies, the crystallites are separated by pores, which are nearly the same size as the crystallites obtained. All three kinds of pore structures have found their own applications

1.3.4 Gravimetric measurement

In addition to its structural morphology, porous silicon is characterized by its porosity. For the portion of monocrystalline silicon concerned by the porosification, this represents the proportion of material removed relative to the initial fraction, i.e. the ratio of the volume of created vacuum over the volume of initial silicon. Moreover, in its most general sense, a "pore" is an engraving pit whose depth exceeds its width **[57]**.

Porosity is most commonly determined by gravimetric measurement and it is calculated by the following formula **[58]**:

$$P(\%) = \frac{m_1 - m_2}{m_1 - m_3} \tag{2.1}$$

Where m_1 (g) is the sample weight before anodization, m_2 (g)sample weight just after anodization and m_3(g) is the sample weight after dissolution of the complete PSi layer. Complete removal of the porous silicon is easily accomplished by chemical dissolution in concentrated potassium (KOH) solution (34%) at room temperature with the use of ultrasound for a few minutes. From these measured masses, it is possible to determine the thickness L of the porous layer according to the following formula:

$$L = \frac{m_1 - m_3}{S \cdot \rho} \tag{2.2}$$

Where ρ ($g.cm^{-3}$) is the density of bulk silicon and S(cm^{-2}) is the area of the wafer exposed to HF during anodization **[57]**.

It should be noted that, when a material is annealed, some pore openings might close, resulting in closed porosity. For gravimetric measurements, if a probe molecule size is smaller than the pore size, then the pore can accommodate the probe molecule and thus the porosity can be measured. Porosity is a macroscopic parameter that does not completely describe the porous material. In order to gain a complete understanding of all the

characteristics of a porous material, it is necessary to consider the morphology of the material as well. It is difficult to systematically characterize the morphology of a PSi layer.

Qualitatively, besides porosity, there is a distinction between the following six parameters: pore shape, pore orientation, shape of the bottom of a pore, fill of macropores, branching and depth variation as shown in Fig. 2.1 **[59]**.

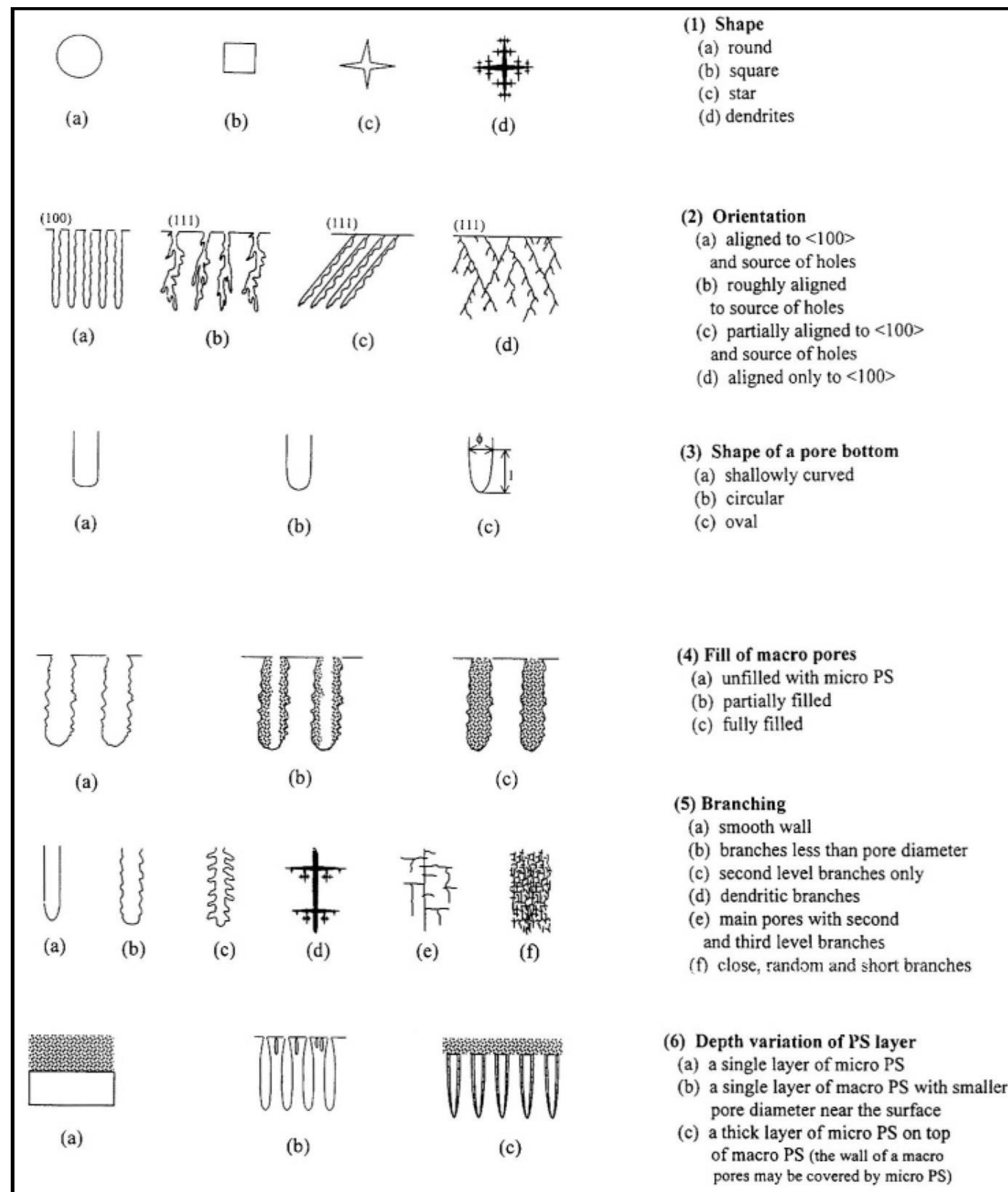


Figure 1.4 Morphological features of Porous silicon **[59]**

1.3.5 Thickness layers

The anodization time is particularly the most important parameter of which the thickness of PSi layer depend. Higher duration lead to thicker PSi layer **[35]**.

Scanning electron microscopy (SEM) measurement is the common technique to measure the layer thickness of PSi material, from this later the etching rates is calculated as shown in equation (2.3).

$$v_{PSi} = \frac{d}{t} \qquad (2.3)$$

Where v_{PSi}(µm/min) is the etching rate of PSi layer, d(µm) is the layer thickness and t(min) is the etching time.

1.3.6 Thermal oxidation of porous silicon

Micro- and meso-PSi can be partly oxidized, by chemical or electrochemical methods, however, these last are not compatible with the microelectronics fabrication methods due to potential contamination issues, but they may offer a good choice for other applications. Many oxidation methods exist, for instance, anodic oxidation in non-fluoride electrolyte, chemical oxidation using HNO_3,O_3, H_2O_2, aging in ambient conditions, thermal oxidation in wet and dry O_2, rapid thermal annealing and nitridization at different temperatures **[60].**

Thermal oxidation is needed to fully oxidize the PSi layer and used in the microelectronic industry to produce high-quality oxides on flat silicon. The difference between these silicon structures is the extent of the oxidation.

A preliminary annealing at low temperatures (up to 300°C) improves the parameters of oxidized PSi. It has been shown that it is not desirable to anneal as-prepared PSi at temperatures that exceed 400°C because it could lead to a drastic restructuring of the PSi layer. Even at low temperatures, surface migration of silicon atoms leads tothe coalescence of pores due to the large surface area **[61].** The desorption of dihydride (Si - H_2) occurs at 300°C and Si - H bonds seem to be stable at this temperature upto around 400°C at which point hydrogen starts to desorb **[62]**. Therefore, pre-oxidation of PSi at low temperatures in the range of 300°C creates anoxide layer along the pore walls, which prevents the restructuring of the sample.

Thermal oxidation of PSi layer allows increasing insulation of the substrate, to ensure high resistivity and low permittivity of this later in RF application. Furthermore, the pores size degrade the properties of the substrate when they are relatively small (a few nm) due to the tunneling effect between the adjacent crystallites. A pre-oxidation in either O_2 or N_2 environment is necessary, it's stabilizes the structure and creates a native oxide in a controlled fashion **[16].**

1.3.7 Applications of porous silicon

According to the literature **[63]**, the applications of porous silicon are grouped into twelve domains: electronics, optoelectronics, optics, diagnostics, energy conversion, catalysis, filtration, adsorbents, medicine, food, cosmetics and consumer care.

In our work, we are particularly interested in the microelectronic field, in terms of the use of the dielectric properties of porous silicon, its implementation was most often done in the form of thick insulating boxes mainly in the field of radio frequencies **[54]**,**[56]**, **[64].** Researchers have demonstrated positive results in reducing losses, improving quality factors for passive inductance devices and abilities on porous silicon **[65]**.

While the SOI silicon substrate offers the possibility of combining high and low resistivity of the materials in a single circuit, one of the main advantages of a porous silicon approach is the possibility of locally defining high resistivity regions in a substrate essentially low resistivity **[66]**.

Recent work on localized porous silicon has been carried out by the team of A. G. Nassiopoulou **[8]**, **[12]**, **[33]**, **[67]**, and that of G. Gauthier **[13]**, **[18]**, **[44]**, **[68].**

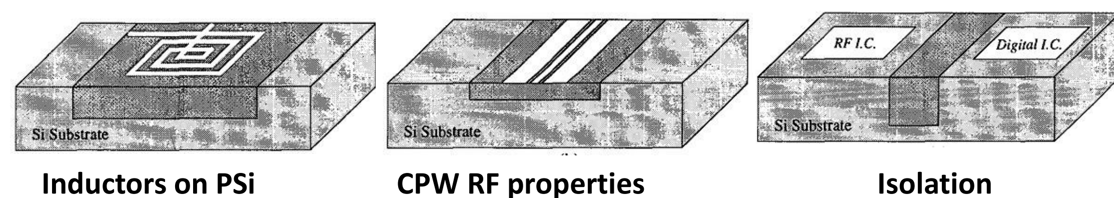


Figure 1.5 Porous silicon technology for RF Integrated Circuit Applications **[65-66]**

1.4 Conclusion

A brief description thus characteristics, advantages and disadvantages of substrates (Standard bulk silicon (Std), High Resistivity (HR), Trap-rich high resistivity (TR) and Porous silicon (PSi)) used in the industry of microelectronics was presented in this first part. The focus is on porous silicon substrate, thanks to its lower permittivity, high resistivity, its morphology and its nano-structuring, which leads it suitability to co-integrate on-chip passive elements and active devices for RF and system-on-chip applications.

The ease of implementation of the electrochemical production process that we will study in Chapter 2, makes porous silicon, a relatively easy material to integrate into the technology related to microelectronics, and at the same time presents a low cost process.

Chapter 2

ELABORATION AND PHYSICAL CHARACTERIZATION OF PSI FOR RF APPLICATIONS

2.1 Introduction

The objective of the work is first to explore the influence of the nanostructure, nanomechanical properties, stress, and roughness of the porous silicon layer through different characterizations methods, then, the relationships between the analyzed structure of the Porous silicon layer versus its electronic properties, as it has been demonstrated in our work[16]. The ease and low cost of obtaining porous silicon and the multitude of its applicable properties make this material a field of radio frequency devices development.

2.2 Elaboration of porous silicon

2.2.1 Experimental setup for the electrochemical etching

Electrochemical etching in a hydrofluoric acid (HF) solution is a well known technique for making different silicon structures for a wide range of applications. The advantage of this method is its simplicity and ability to anodize silicon-on-insulator structures, the simplest way to realize an electrochemical cell is to immerse two connected electrodes within an electrolyte. One electrode supplies electrons to the solution (the cathode), where the reduction takes place. The other one removes electrons from the solution (the anode), where the oxidation is occurring. The current supply is provided by the current source which is driven by a potentiostat. The whole system is ultimately controlled by a computer. There is more than one way to organize an electrochemistry experimental setup for PSi, and various methods have been described in the literature, such as, the immersion cell**[69]**, the O-Ring cell **[35]**, the double cell **[70],** cell with electrolyte circulation **[60],** etc.

The design of the anodizing tool depends largely on the nature of the application, the type of layers and the flexibility of the required process, the proposed flow and the degree of automation. The electrolytes used for the anodic etching process are based on a mixture of hydrofluoric acid (HF) and ethanol. Silicon wafers (100) of p-type with different resistivity (5-20 mΩ-cm), (1-10 Ω-cm) and (10-25 Ω-cm) were used as substrates for anodizing the porous silicon, an Ohm contact was made through the deposition of a 200 nm layer of aluminum behind the wafers. Adhesive tape was used to mask the entire substrate with the exception of the area where the anodizing and plating were performed as shown in Figure 2.1. The sample was mounted in an electrochemical cell connected to a potentiostat -galvanostat PAR 362. In the case of our application, the surface of the silicon wafer required pre-cleaning before the anodization, to remove the native oxide film, which cover the surface wafer. The oxide layer will be removed when the wafer is immersed in two successive cleaning baths of the solution (H_2SO_4 + H_2O_2) and then in the HF. Distinct morphologies of meso and micropores were obtained as a function of doping of the Si wafer as well as by the change of the electrochemical parameters.

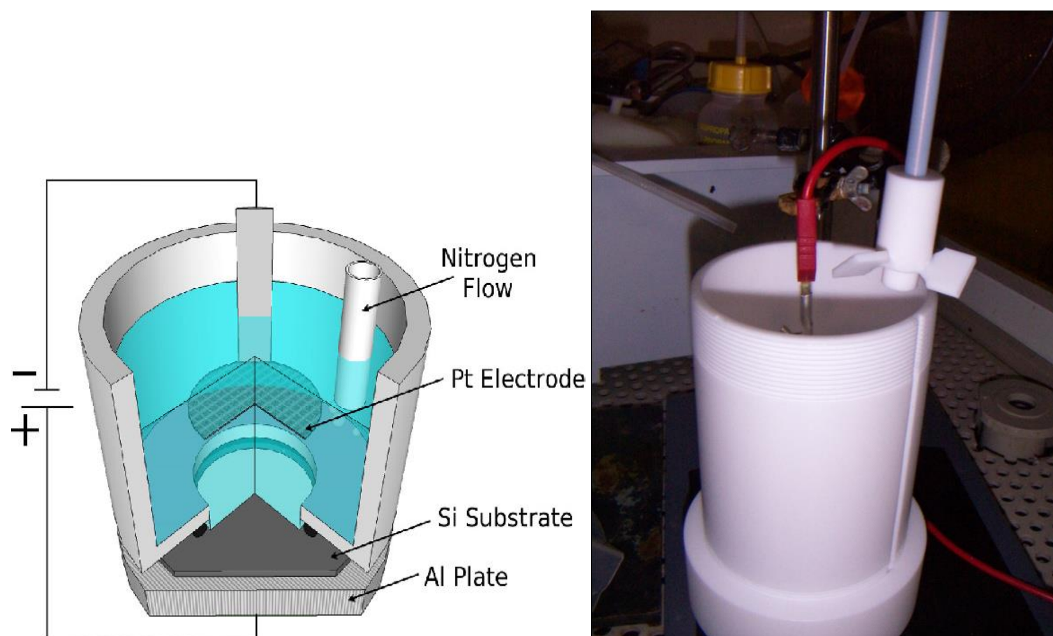


Figure 2.1 Electrochemical cell used for the anodization

The choice of cell materials depends on the targeted electrolyte. Since HF based electrolytes are widely used in the electrochemistry of silicon, materials resistant to HF must be used PVC(polyvinyl chloride), PP (Polypropylene), PTFE (polytetrafluoroethylene) and

PVdF (Polyvinylidene fluoride) are all used, with PVC being superior because it is inexpensive, inert in HF and it has good mechanical performance **[35].**

2.2.2 Porous silicon anodization parameters

For the manufacture of a microporous layer structure on Si substrate with resistivity of (1-10 Ω.cm), a HF : ethanol based electrolyte and a current density of 10 $mA.cm^{-2}$were applied during the etching process to obtain a porous thickness of 2 μm to 200 μm related to an etching time ranging from 250 s to 24000 s, respectively. All specimens were made in the dark on an electrochemical etching platform inside a fume hood at room temperature (18 ± 1°C). Finally, the samples were rinsed in deionized water and dried with a stream of nitrogen.

The relevant parameters which influence the formation process are summarized as fellow:

- Substrate doping
- Wafer type and resistivity;
- Current density;
- HF concentration in electrolyte;
- The used Solvent; lowering the surface tension with, for example, the use of ethanol, allows hydrophobic porous silicon to be more wet enabling higher homogeneity;
- Etching time;
- Temperature and ambient humidity;
- Drying conditions

Once a porous layer is formed, no more electrochemical etching occurs in that layer.This creates the possibility to change porosity as a function of depth.

2.3 Morphological characterization of porous silicon

The condition to produce high performance RF devices is always related to the surface state (structure) of substrate. Then, it is important to study its structural and mechanical properties before and during the different steps of the post-anodization process of silicon. Consequently, an important number of articles are devoted to the mechanical properties of Si bulk substrate **[71-73].** In the other hand, many works concerning the morphology and structural properties of Porous silicon have been performed **[19], [74-75].**

The stress and roughness in porous Si could affect the integration of porous Si devices in microelectronic integrated circuits based on silicon.We investigate the nanomechanical properties and the structure analysis of the porous silicon layer with different thicknesses formed on p-type Si substrate with two resistivities. The formed PSi layers are characterized by Scanning electron microscopy (SEM), Atomic force microscopy (AFM), and Nanoindentation.

2.3.1 Scanning Electron Microscopy (SEM) analysis

For any application of the porous Si a morphological characterization is of prime, a field emission scanning electron microscope (FE-SEM, GEMINI Ultra 55 Zeis) under 3 keV electron acceleration voltage is used in order to measure: the thickness of the porous silicon, the size of the pores and the crystallites. The sample PSi-M with 50 µm thickness of a mesoporous layer is obtained after anodization of p-type Si (ρ=5-20 mΩ.cm)in (50%) HF: ethanol (1:1), at current density of 75mA/cm^2 during 40 min. Figure 3.2 shows the cross-sectional and top view SEM images of the mesoporous layer with pores varying from 10 to 12 nm. On the other hand, standard p-type (ρ = 1-10 Ωcm) sample (PSi-S) is exposed to an electrolyte based on (2:1) mixture of (50%) HF and ethanol, and the anodization is conductedat a current density of 10 mA/cm^2 during 100 min for 50 µm thickness of porous layer.A spongy structure with pores diameter ranging from 1 to 5 nm are obtained as shown in Figure 2.2. The depth of the pores can be varied depending on the time period of the electrochemical process. In the present work, the thickness of the porous silicon layer is about 50 µm for the two types of wafers doping.

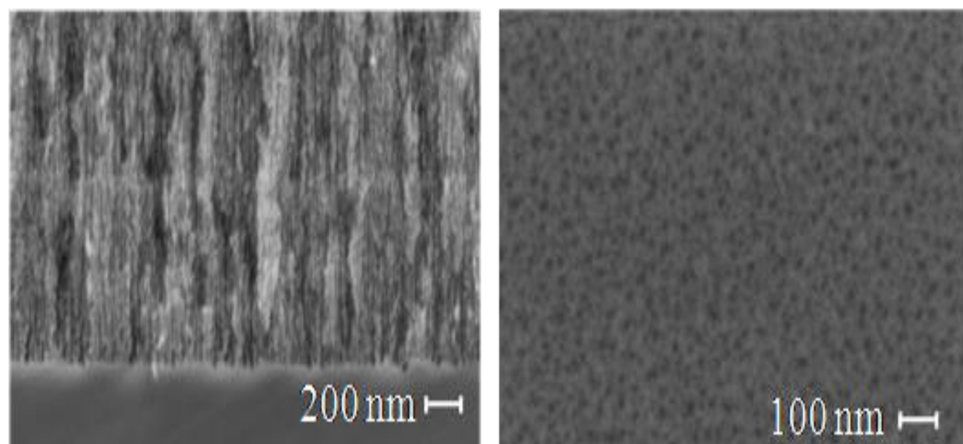


Figure 2.2 Cross-sectional SEM image (left) and top view (right) of mesopores obtained after anodization of highly doped P-type Si (ρ= 5-20 mΩ.cm)

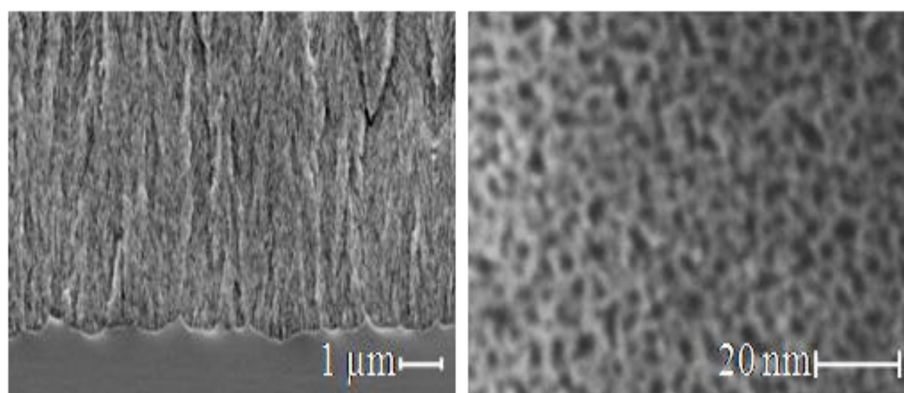
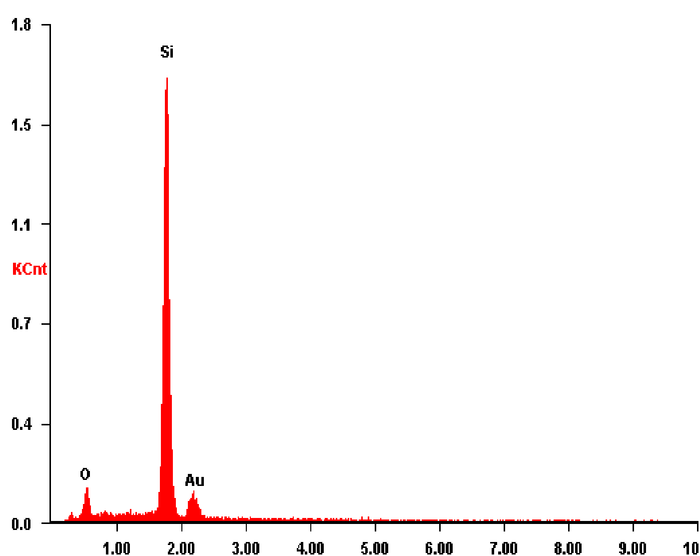


Figure 2.3 Cross-sectional SEM image (left) and top view (right) of mesopores obtained after anodization of standard P-type Si(ρ = 1-10Ω.cm)

The microporous silicon layer after oxidation is characterized by Energy Dispersive Spectroscopy (EDS), this later is a chemical microanalysis technic which is used in conjunction with scanning electron microscopy (SEM)

The recorded energy dispersive spectroscopy analysis spectrum reveals the presence of oxygen after oxidation through the whole layer thickness and into the filled pores indicating that the sample contains silicon and oxygen. The average compositions of the anodization and oxidation have been estimated quantitatively with values of 84% for Si and 16% for O within the anodized layer as shown in Figure2.4.



Element	***Wt%***	***At%***
O K	09.92	16.21
SiK	90.08	83.79

Figure 2.4 Energy dispersive spectroscopy (EDS) spectrum of porous silicon layer after oxidation

2.3.2 Porosity

A mesoporous layer structure of the PSi-M substrate is obtained with an estimated porosity of 50 % for PSi 50µm thickness, and about 44 %for the 10µm PSi thickness. The variation in porosity with thickness is related to the chemical dissolution of the porous material during its formation. According to results of R. Herino et *al*[76], who studied porosity as function of the thickness, their work summarizes that the porosity and pore sizes increase with an increase in forming current density or a decrease in hydrofluoric acid concentration. One can conclude that for PSi-M substrate the porosity increase with the increasing of thickness and for a same thickness (50µm), the porosity increases with the increase of the resistivity, as it shown in (Fig. 2.5).

On the other hand, the same observation is made for PSi-S substrate, where the porosity increases with thickness until reaching saturation, which seems to be the highest porosity of 65% for 50µm thickness as it is shown in Fig. 2.6. Thereafter, the PSi develops cracks and small pores start growing. All results corresponding to the two nominal resistivities are summarized in Table 2.1.

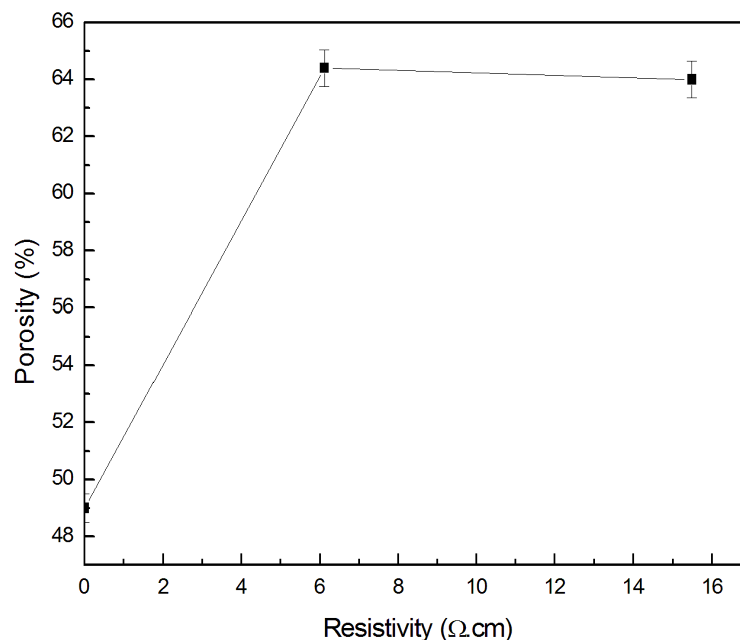


Figure 2.5 Porosity vs resistivity for 50µm of porous silicon

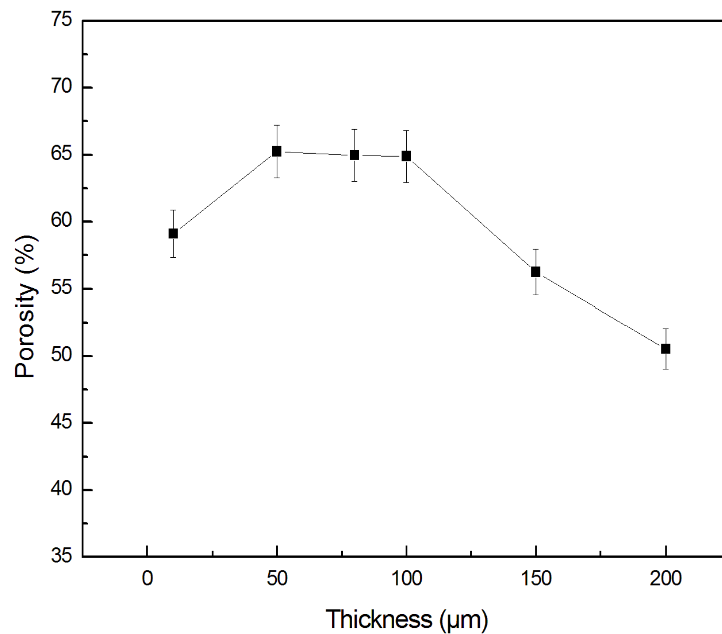


Figure 2.6 Variation of porosity with thickness for PSi-S

Nominal resistivity (Ω.cm)	Porous thickness (µm)	Pore size (nm)	Porosity (%)
0.005- 0.02	50	10 - 12.5	≈50
1-10	50	1 - 5	≥ 65

Table. 2.1 Comparison between two nominal resistivity

2.3.3 Atomic Force Microscopy(AFM)analysis

The porous silicon layer obtained after anodization and oxidation must have similar characteristics to that of monolithic silicon to withstand of a standard process in microelectronics (deposits, etching and high temperature annealing) until devices integration. In this context, the morphology, the roughness and the spectral analysis of the porous silicon layer were characterized by Atomic force microscopy (AFM Agilent 5500).

From atomic force microscopy image (Fig. 2.7), a change in the porous silicon structure is observed, for a PSi-S substrate (1-10 Ω.cm), the size of pores and crystallites increase with PSi thickness.

Figure 2.8 presents the superposition of power spectral density versus spatial frequency for different thicknesses of PSi, 5µm, 10µm, 50µm and 200µm. At the lower spatial frequency, a flat curve with a constant value is observed for all PSi thicknesses except for 200 µm thickness a significant variation of the power spectral density is shown .

Figure2.9 shows at small-scale, a roughness which is quite identical regardless the thickness of the PSi layer. However, at large-scale the roughness increases with the thickness of the PSi layer. The RMS (*Root Mean Square)* roughness becomes constant above 100 nm scan, this indicates, that is necessary to scan at least 100 nm to avoid losing information on the surface roughness.

RMS roughness and correlation length as a function of the thickness are extracted as it is shown in (Fig. 2.10). RMS is the root mean square average of the profile height deviations from the mean line, recorded within the evaluation length; the correlation length ξ is the typical distance between two different irregularities (or bumps) on the surface, which increases with increasing thickness of porous silicon. According to the Table 2.2, rough surface when values close to 1 indicate a smooth surface **[75, 77]**

From this results, we can conclude that the porous layer due to the electrochemical etching of silicon surface leads to an increase of the surface roughness, despite this, the roughness reach 0.9 nm for 50µm, so the surface of PSi still smooth, it is 2.5 nm for 200µm thickness of PSi. In the other hand the correlation length, remain fixed until 50µm thickness of PSi. Therefore, one of the main benefits of the porous silicon substrate compared to the silicon is having a rougher surface with large specific surface.

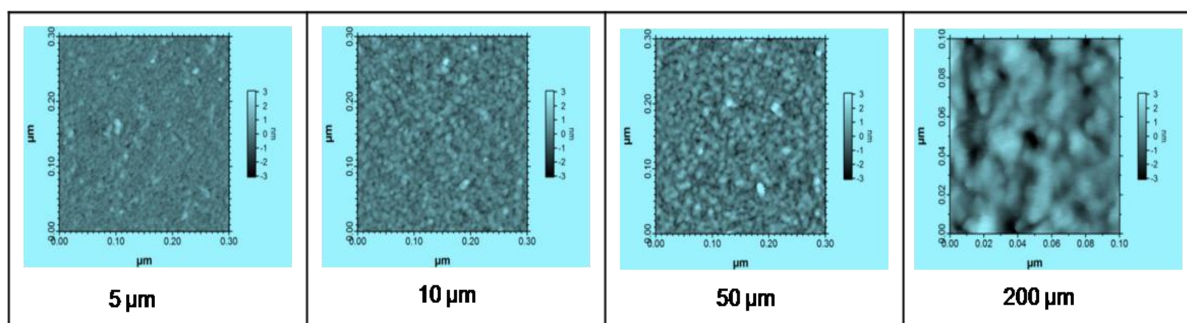


Figure 2.7 AFM image of different thickness of PSi-S substrate (1-10Ω.cm)

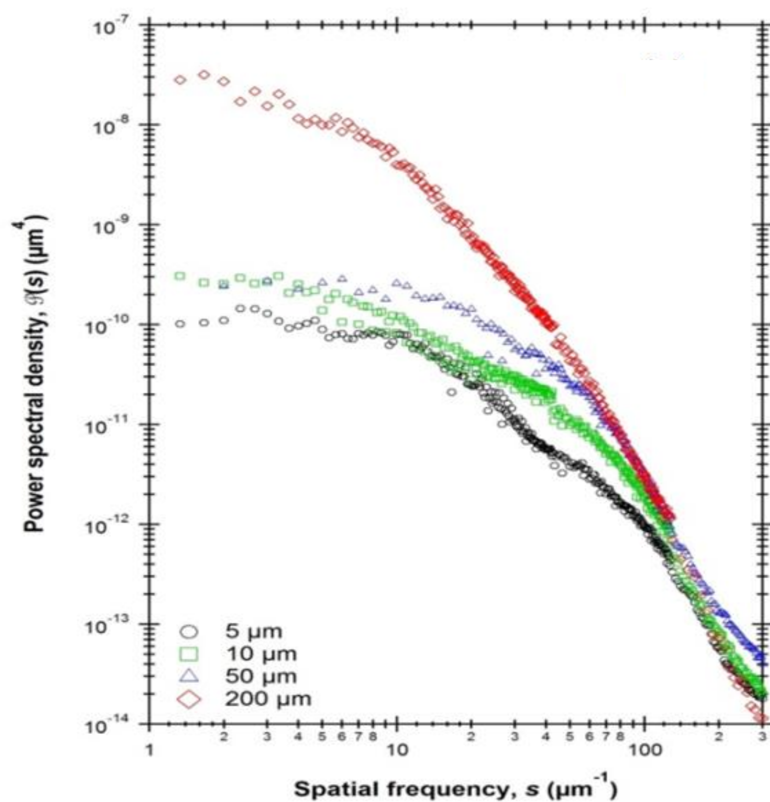


Figure 2.8 Superposition of power spectral density vs spatial frequency of (5μm, 10μm, 50μm and 200μm) thickness of PSi-S substrate

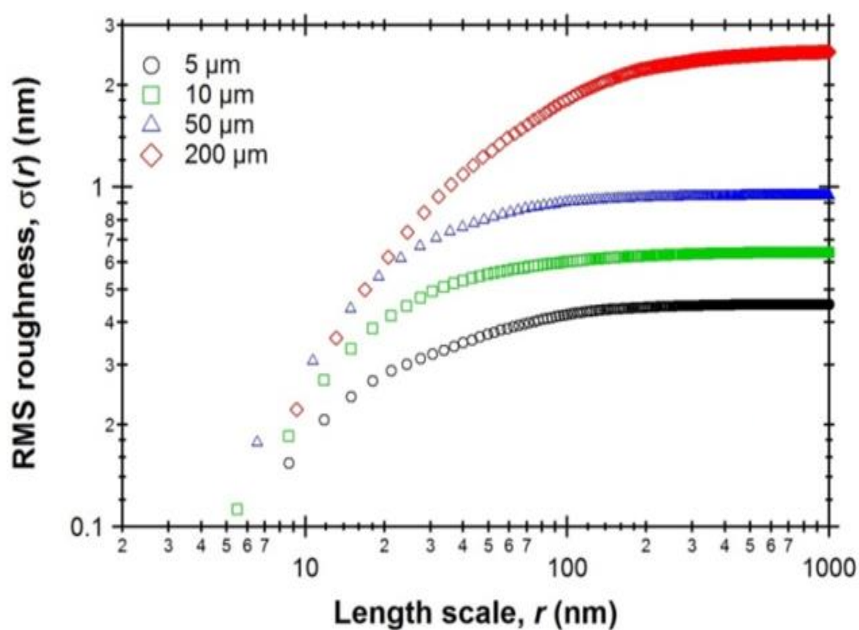


Figure 2.9 Superposition of RMS roughness vs length scale of (5μm, 10μm, 50μm and 200μm) thickness of PSi-S substrate

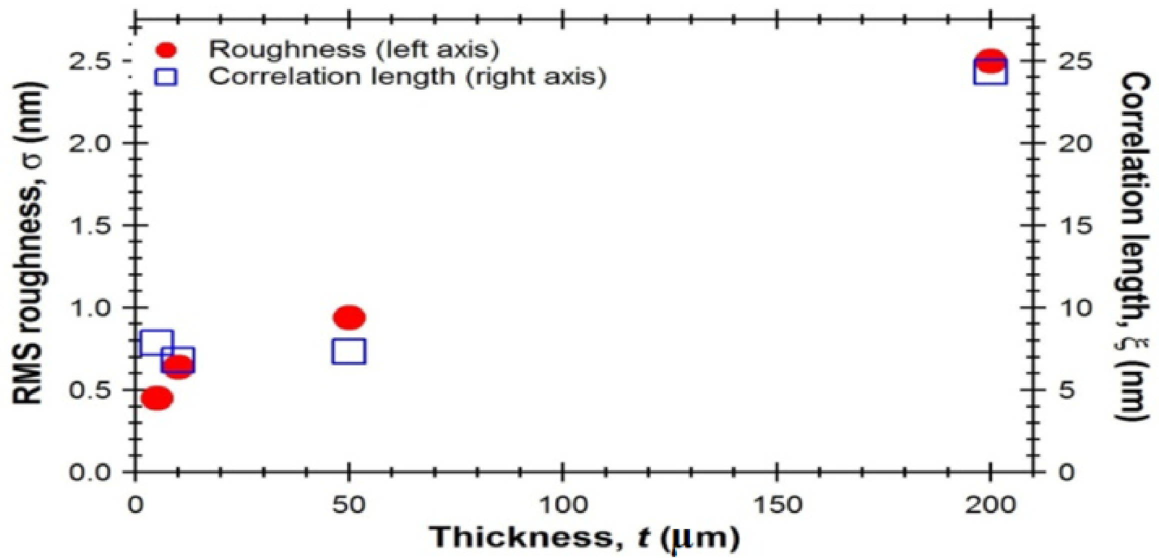


Figure 2.10 RMS roughness and correlation length vs thickness of PSi-S substrate

PSi thickness (μm)	σ (nm)	ξ (nm)
5	0.45	7.5
10	0.65	7.5
50	0.9	7.5
200	2.5	24

Table. 2.2 Roughness (σ) and correlation length (ξ) corresponding values of different thickness of PSi-S

Regarding to the previous results, the PSi-S 50 μm seems have surface roughness less than 1 nm, for that we investigated two different resistivity for the same thickness of porous silicon. In the figures 2.11 the effect of substrate resistivity is highlighted by the surface morphology of PSi, where the substrate PSi-M present large pores size. Through the roughness of PSi-M, which is two times greater than that of PSi-S (Fig. 2.12) the PSi-S substrate, give better results comparing with the PSi-M. The SEM results are confirmed by the AFM analysis, the SEM and AFM are complementary analysis.

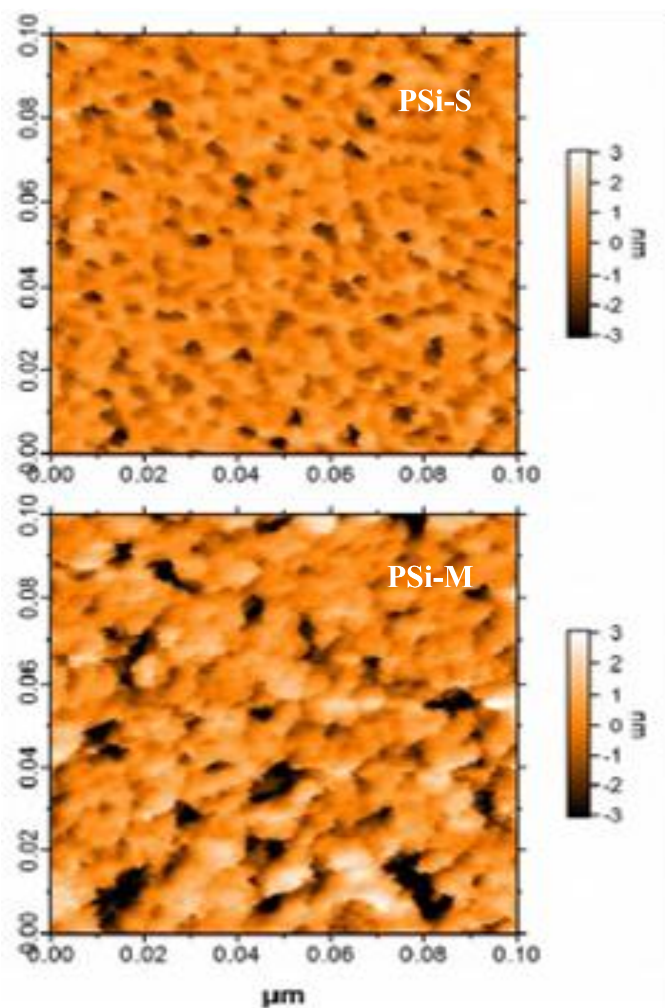


Figure 2.11 AFM image of PSi-S and PSi-M with the same thickness 50µm of porous silicon

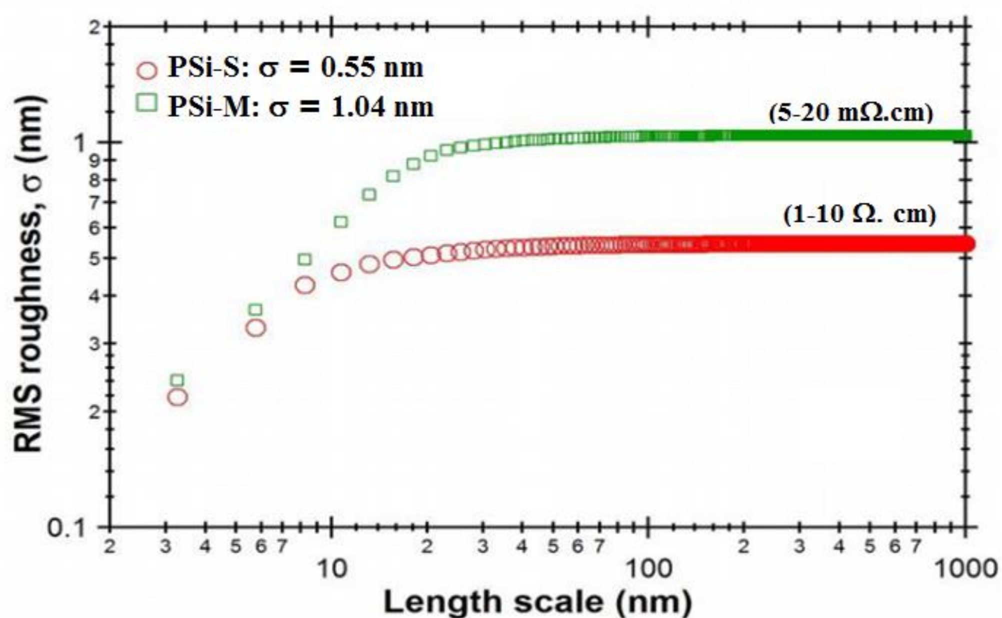


Figure 2.12 RMS roughness for two resistivity used

PSi-S (1-10 Ω.cm) and PSi-M (5-20 mΩ.cm) with the same thickness 50µm of porous silicon

2.4 Optical characterization of porous silicon

The Fourier Transform Infrared Spectroscopy (FTIR) measurements allow us to follow the evolution of the absorbance spectrum of oxygen versus time due to the oxidation of the samples. S. Gardelis, AG Nassiopoulou et *al* **[78]** used Transmission Electron Microscopy (TEM) and Fourier Transform Infrared Spectroscopy (FTIR) to characterize silicon nano-pores (1.5 - 7nm) after laser irradiation for photonic applications.

Thermo-Nicolet Nexus 670 Fourier transform infrared spectrometer was used to characterize the bonding properties of porous silicon layer. The infrared spectra were measured in absorbance mode and were referenced against a single silicon crystal sample. Figure 2.13 shows the IR spectra of PSi layer, it show a small peak at about 1100 cm^{-1}, corresponding to the stretching vibration of Si-O bond(oxygen present in interstitial sites in the silicon crystal lattice).A periodicity is observed, which is due to interference phenomena in thin layers. Porous silicon is commonly highlighted by the stretching vibrations of Si-H, $Si\text{-}H_2$ and $Si\text{-}H_3$, respectively, at 2087, 2110, and 2140 cm^{-1}**[78-80].**Furthermore, other modes have been observed such as scissor bending at 915cm^{-1} of the $Si\text{-}H_2$ bond and at 626 cm^{-1} from bending mode of the Si-H bond. The torsional and the rotation modes have also been observed at 665 cm^{-1} and at 512 cm^{-1}, respectively **[80].**

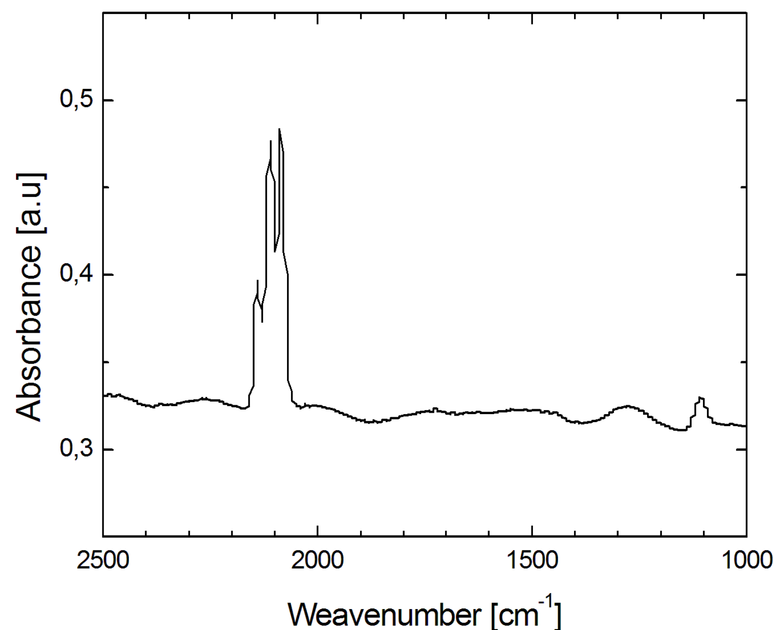


Figure 2.13 FTIR Spectrum of porous silicon layer before oxidation

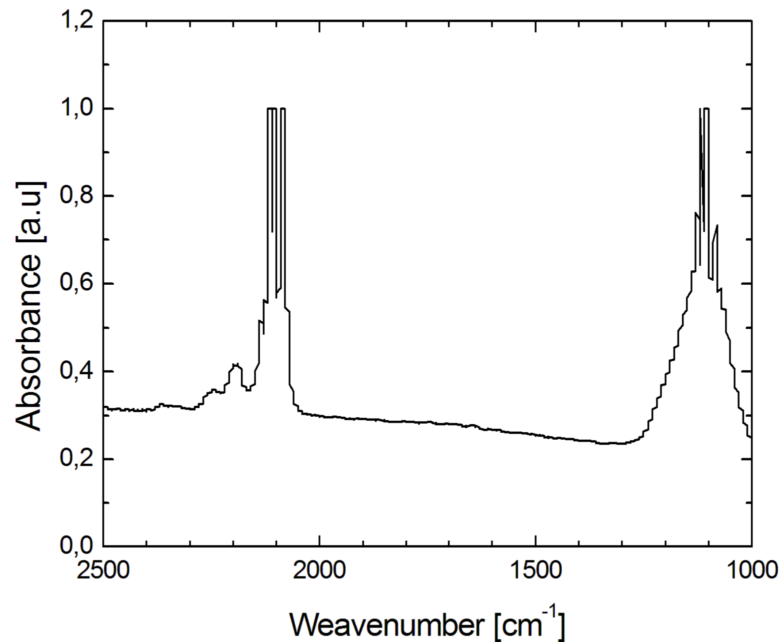


Figure 2.14 FTIR Spectrum of porous silicon layer after oxidation

Figure 2.14 presents the FTIR spectrum of the sample after oxidation. Besides the porous silicon peaks, a strip of significant vibration of Si-O bond **[81-82]** containing the vibration of symmetric and asymmetric stretching modes of Si-O-Si at, respectively, 1073 cm^{-1} and 1169 cm^{-1}. A wide band at 1084 cm^{-1} and two simultaneous peaks at 1100 cm^{-1} and 1124 cm^{-1} corresponding to the stretching vibration of Si-O-Si bond. Another peak occurs at 800 $cm^{-1}$and 869 cm^{-1}correspond to the deformation vibration mode of O_n-SiH_x. Low intensities of peaks that appear at 2196 cm^{-1} and 2256 cm^{-1} are assigned, respectively, to the stretching vibration of O_2Si-H_2 and O_3Si-H bonds **[80]**.

Finally, the superposition of the two spectra in Figure 2.15 highlights the oxidation of porous silicon with intense peaks.

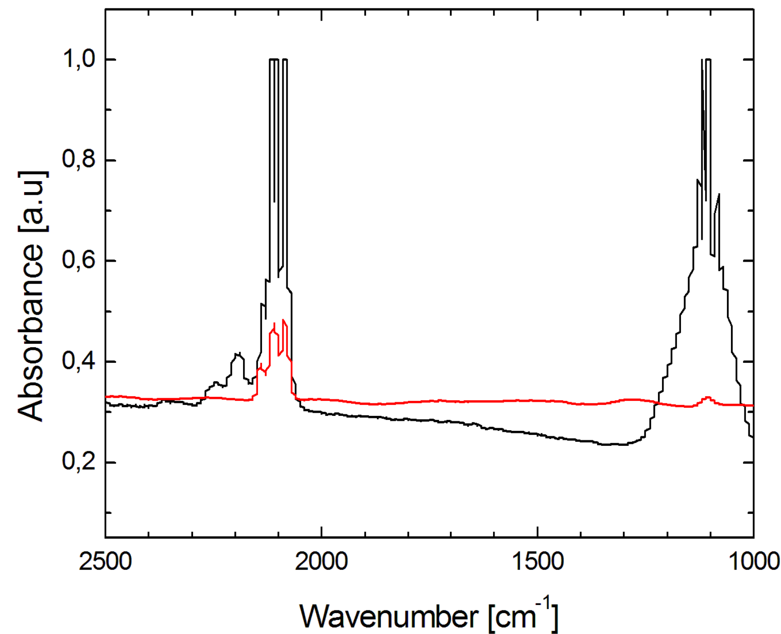


Figure 2.15 Superposition of FTIR spectra of the 50 µm porous Si film after oxidation

2.5 Mechanical characterization of porous silicon

2.5.1 X-ray diffraction (XRD) analysis

X-ray diffraction allows the study of crystalline deformations in porous silicon. As an example, Figure 2.16 represents the high resolution X-ray diffraction profile obtained on a mesoporous silicon sample,the knowledge of the variation of the porous silicon mesh parameter associated with the measurement of the radius of curvature, enables to estimate the Young's modulus and the Poisson's ratio **[83].**

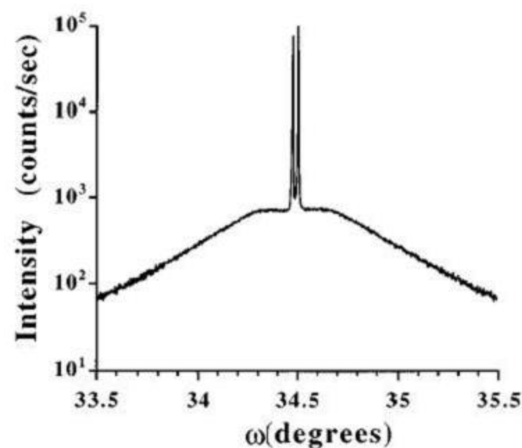


Figure 2.16 High resolution XRD profile obtained on a mesoporous silicon sample with a 65% porosity **[83]**

In order to reduce the mechanical constraints in porous silicon and gain good electrical isolation between metallic devices and the porous Si layer, it is necessary to oxidize at least partially the porous silicon substrate. XRD spectra analysis were done with CuKα radiation (1.54 Å) using a D8 Advance Bruker diffractometer. The XRD spectra of the porous Si p-type layer before and after oxidation are shown in Figure 2.17 and 2.18 with each Bragg peak, assigning its identification and Miller indices. We notice the appearance of a peak on the left of the spectrum in Figure 3.18, which not exist in Figure 3.17, confirming the oxidation of PSi and indicating that is an amorphous oxidation of the porous silicon, while the (400) plane of the silicon peak does not change.

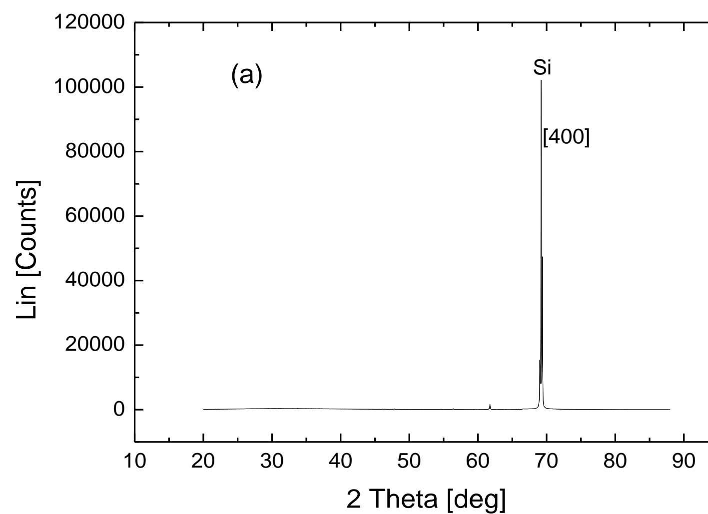


Figure 2.17 X-ray diffraction spectrum of porous Si (100) p-type before oxidation

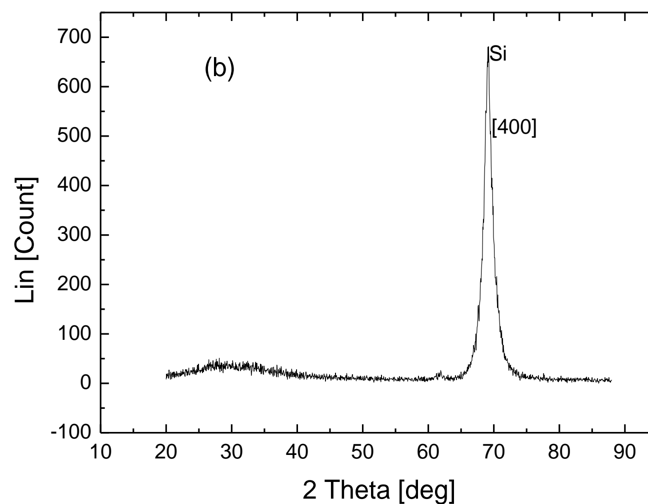


Figure 2.18 X-ray diffraction spectrum of porous Si (100) p-type after oxidation

2.5.2 Measurement of Young's modulus and hardness

From the pyramidal fingerprints obtained by the hardness test, it is possible to extract characteristic Vickers hardness values from nano or mesoporous silicon, therefore, Duttagupta et *al* extracted Vickers hardness values **[84].** On the other hand, Bellet et *al* have been able to go back to Young's modulus values from the same type of experiments **[85].**

The hardness and elastic modulus were measured using Agilent Nano Indenter G200 system equipped with a Berkovich indenter by the load–depth-sensing nanoindentation method. Its standard configuration utilizes the Agilent XP indentation head, which delivers less than 0.01 nm displacement resolution, 500mN maximum charge and 500 µm maximum indentation depth.

To minimize the effect of the ductile substrate and avoid the influence of the substrate, a limit load of 50mNwas applied depending on thickness of porous silicon and the penetration depth limit was 2500 nm. For each sample, 16 indentation tests were performed to obtain the mean value and the standard deviation (see Fig. 2. 19). The measurement errors did not exceed 3%. The hardness was calculated according to the Oliver–Pharr method as an average from 16 indents **[86].**

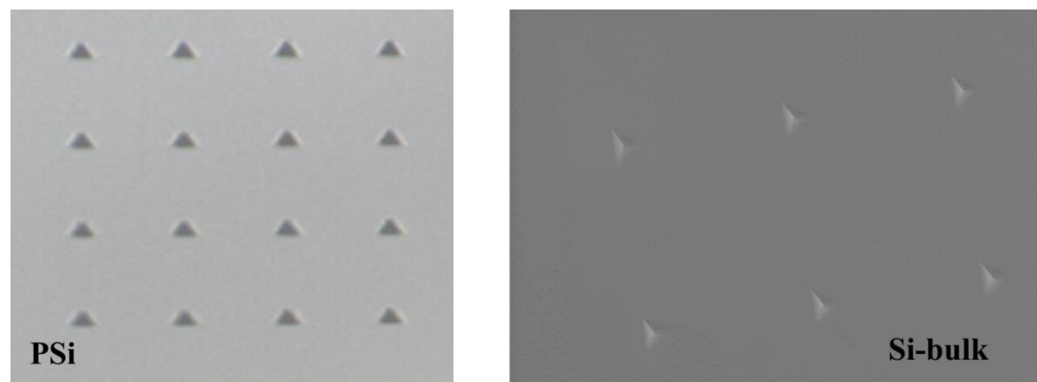


Figure 2.19 Pyramidal fingerprints obtained by the hardness test on PSi and Si-bulk

Before starting to measure the Young’s modulus (E) and hardness (H) of PSi, it is important to measure the same parameters as those of bulk silicon, as it was measured by Nanoindentation in figures2.20 and 2.21the average modulus of Si bulk substrates (ρ = 1-10 Ω.cm) is about 171.2 GPa with an average hardness of 12.3 GPa. These results fit well with those of Ref**. [75].**

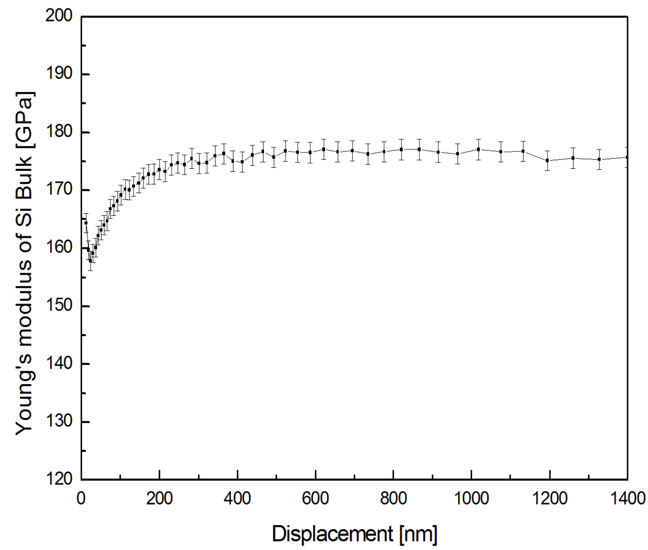


Figure 2.20 Variation of Young's modulus vs displacement in bulk silicon

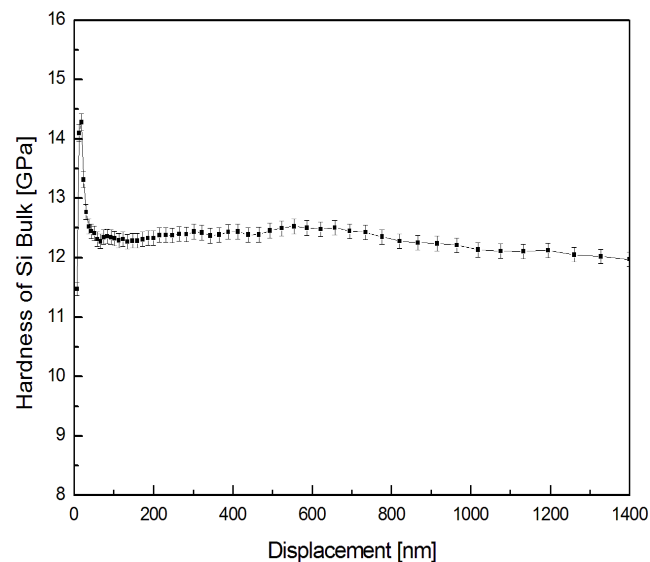


Figure 2.21 Variation of Hardness vs displacement in bulk silicon

Figures 2.22 and 2.23 compare the E and H of five PSi-S samples with spongy structure for different thicknesses reveals very low H and E values (e.g. for 50µm PSi~ 95%) than the value of Si bulk. It is observed that, at the shallow indentation of surface, between (5µm, 10µm) and (100µm, 200µm) samples, the values of H and E have respectively ~ 10% and 7% difference, but for the 50µm sample the value of H and E are in the middle ~50% difference. When tip exceeds 50 nm penetration depth a slight difference is observed for all the samples in H and E values. At early stage, an increase in hardness versus contact depth is observed until the hardness reaches a maximum value due to the finite value of the real tip **[87].**

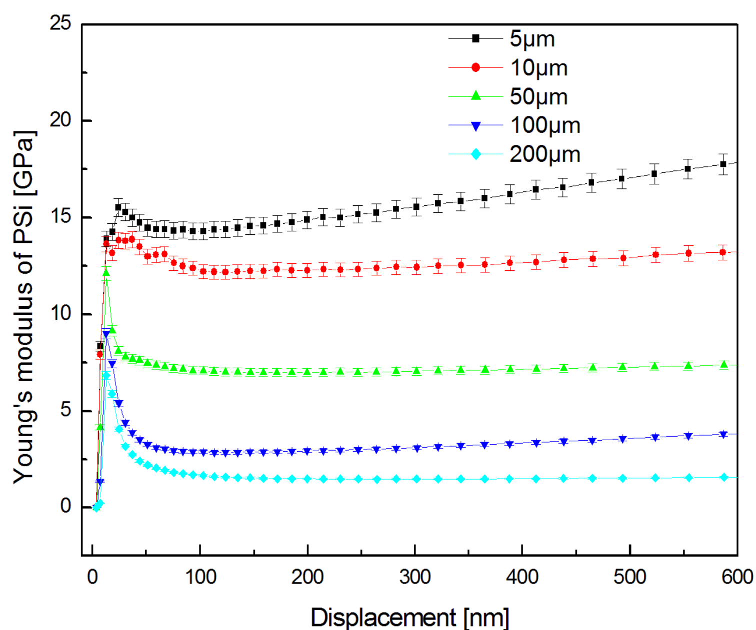


Figure 2.22 Variation of the Young's modulus vs displacement
in porous silicon for different thickness of PSi

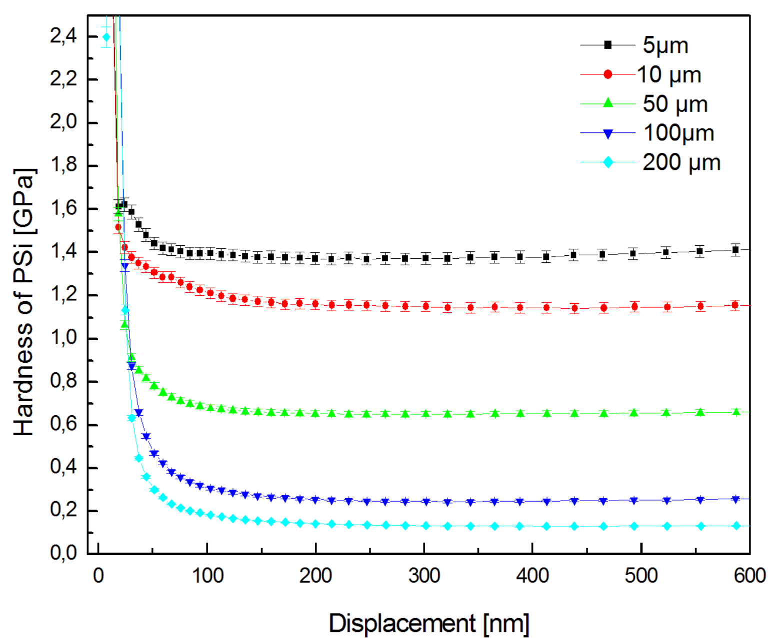


Figure 2.23 Variation of the Hardness vs displacement
in porous silicon for different thickness of PSi

Figures 2.24 and 2.25 show that the H and E decrease with the increase of PSi thickness, which is less stiff than bulk silicon (with lower Young's modulus values), this is due essentially of the porosity of different thickness samples.

The porosity and the thickness of porous silicon could explain this behavior. Indeed, as the thickness of the PSi layer increases, the porosity decreases. For thicknesses greater than 50 µm of PSi, the etching time increases, so that part of the fluorine molecules existing in the solution, will find a difficulty to penetrate through the pores, already formed of the porous layer to reach Si bulk, then these molecules will stay on surface of the PSi layer which will undergo second time the etching, finally, the layer surface of PSi will have the shape resembling waves on the sea.

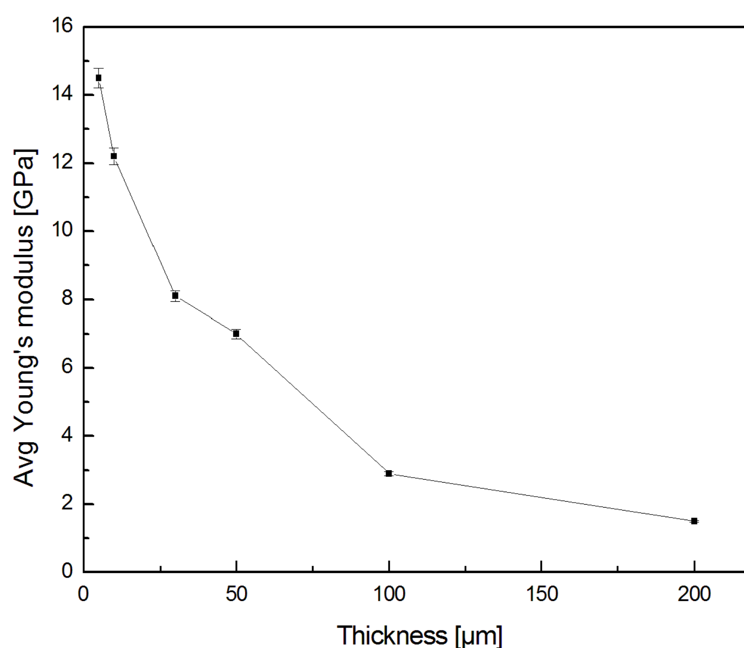


Figure 2.24 Variation of average Young's modulus vs thickness of porous silicon

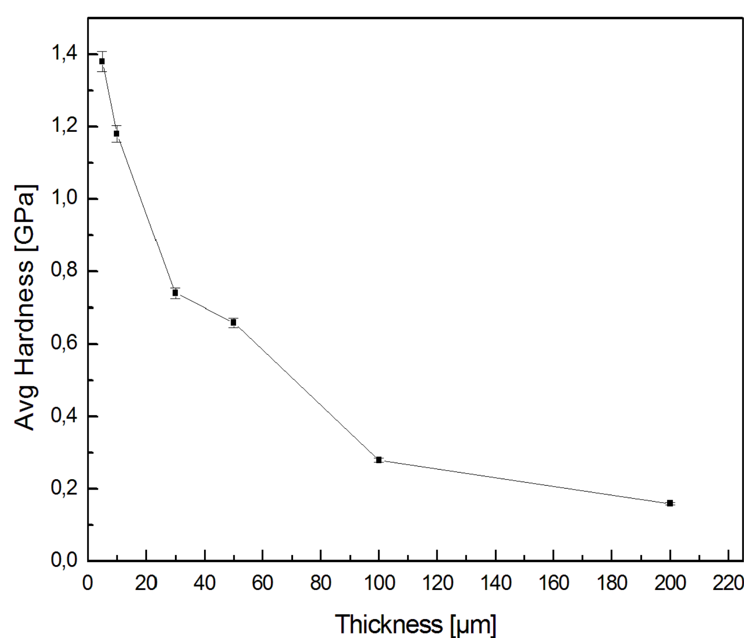


Figure 2.25 Variation of average hardness vs thickness of porous silicon

The sample 50 µm thickness of PSi which have maximum porosity present an average hardness value of 0.7 GPa, a comparison is made for this thickness between PSi-S and PSi-M samples. As it is shown in Fig. 2.26 and 2.27, the resistivity effect on the E and H values of the PSi-M sample is considerable, since their values are 3 times greater than those of PSi-S, probably due to its lower porosity (50%). For PSi-S sample, an increase in Young's modulus is initially observed until reaching a stable value of ~10 GPa whereas, H value tend to decrease to attend1 GPa. However, PSi-M sample reveals greater values, which initially increases and reach a steady value of E ~ 43.5 GPa and H ~3.3 GPa, for both samples they are harder than those comparing in literature **[75], [88-89].**

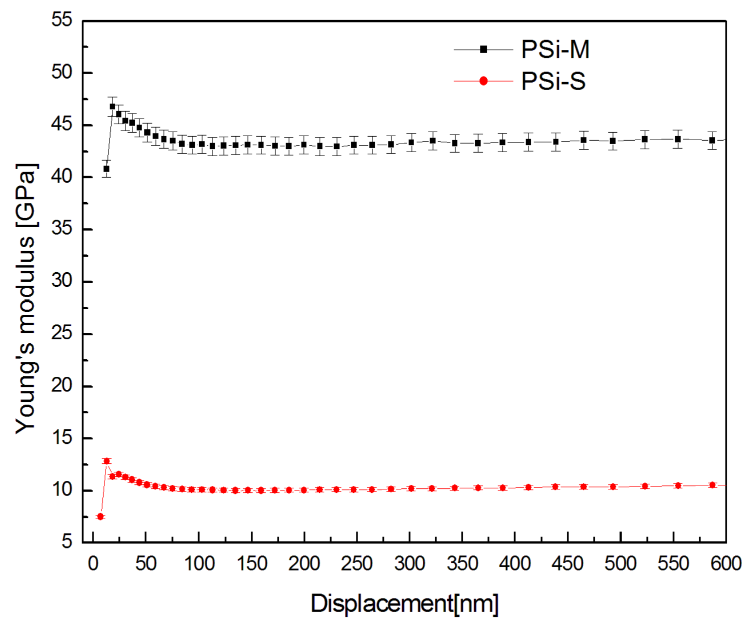


Figure 2.26 Effect of resistivity on Young's modulus

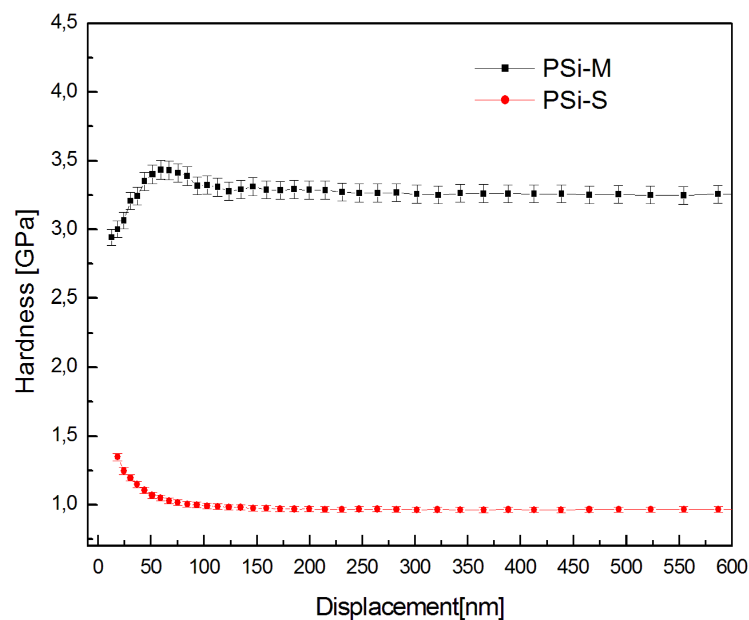


Figure 2.27 Effect of resistivity on Hardness

In order to determine the limit of elastic behavior in a surface contact, the H/E ratio is considered as the most precise measure, which is important for the avoidance of wear **[90]**, related to the elastic strain to failure capability of material **[91]**.

Figure2.28 presents the *H/E* ratio for two samples. It can be observed that the *H/E* ratio for the PSi-S sample decrease from ~ 0.108 at low penetration depth and then it is constant ~ 0.095 up to 100 nm depth. However, the *H/E* ratio for the PSi-M sample increases from ~ 0.064 and up to 100 nm depth it is constant ~ 0.077, at this point the transition from elastic area to plastic deformation of the material is marked. This behavior indicates higher wear resistance of PSi-S compared to the PSi-M sample. Those results are in agreement with **[75, 88]**.

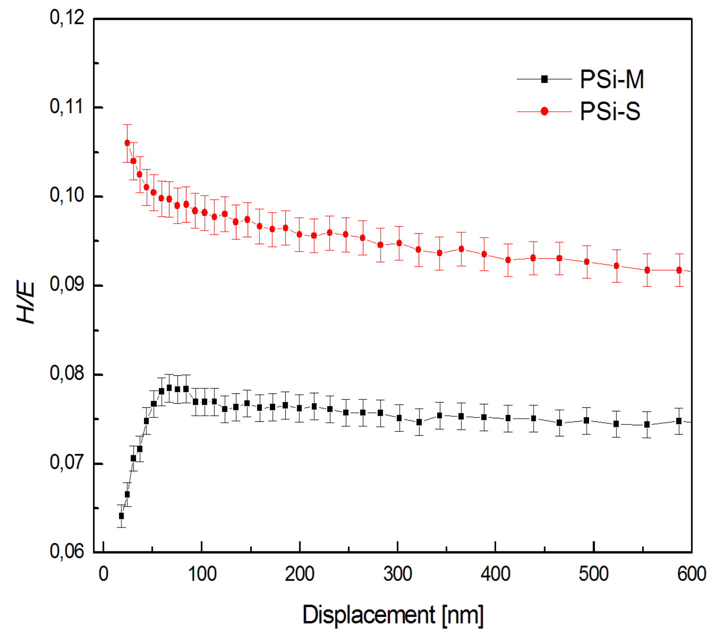


Figure 2.28 *H/E* vs. displacement for PSi-S and PSi-M samples

2.5.3 Stress determination

The stress of different thickness of porous silicon were deduced from stoney's formula (Eq.2.1) after measuring the radius of curvature using an Alpha-Step profilometer by taking average measurements.

$$\sigma \approx \frac{E_{Si}}{6(1-\gamma_{Si})} \frac{t_{Si}^2}{t_{PSi}} \left(\frac{1}{R_1} - \frac{1}{R_2}\right) \tag{2.1}$$

Where σ (GPa) is the stress of the porous silicon film, after anodization, or after annealing, E_{Si} Young's Modulus of silicon substrate (171.2 GPa), γ_{Si} Poisson's ratio (0.22),

t_{Si} thickness of silicon (381±20µm), t_{PSi}(µm) thickness of porous silicon film, R_1(µm) radius of curvature of the silicon substrate before anodization or annealing, R_2(µm) radius of curvature of the silicon substrate after anodization or annealing.

The measurements revealed that the stress values of PSi layers are negative, which leads to a compressive stress, and that this stress increases with increasing thickness of PSi and so, it decreases with increasing porosity, as it observed according to Sun et *al*[88].

The wafers with the high value of the radius curvature could influence the stress measurements in bad way if the devices are integrated on porous silicon, for this reason we have chosen the wafers with the low radius of curvature in order to minimize the stress of wafers. In contrast, the stress is considerably reduced when the thickness of PSi decreases and attain the value of -20 MPa for 50 µm thickness PSi after anodization (Fig.2.29).

Indeed, as it is depicted in Fig. 2.29 the stress decreases for all PSi thicknesses after the annealing process comparing to the stress after anodization. The effect of annealing make the compressive stress decreasing on PSi surface, due to the structural changes, which is caused by the pore size reduction. However, for a PSi thickness of 200µm the layer was cracked, because it cannot support the annealing process. We can also note that during the drying process these stresses can reach tens of MPa, which can lead to cracking too.

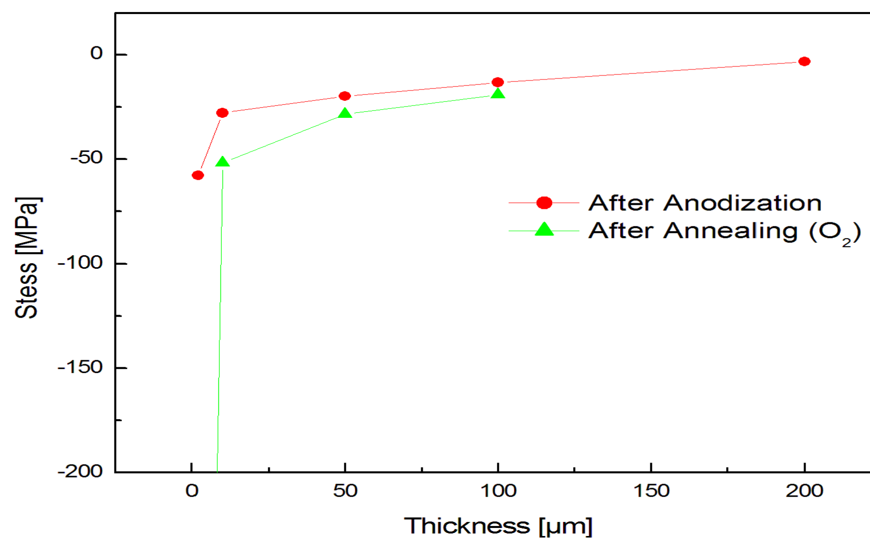


Figure 2.29 Stress varition vs thickness

2.6 Conclusion

Porous silicon is already commonly used to make chemical sensors. Due to its large surface area, it has the advantage of being easily integrated into the usual microelectronic manufacturing processes **[90]**.

In the recent years, special attention has been devoted to the development of microelectronic. Micro and nanostructures based on porous silicon have been used in research fields.

In this chapter, for different thickness of PSi , thanks to SEM and AFM analysis, pore size, porosity and roughness have been determined, as is the case for nanomechanical properties including, nanoindentation and stress. The oxidized layer of PSi was analysed by FTIR , X-ray diffraction, and Energy Dispersive Spectroscopy (EDS). All of these analysis allowed us to choose the appropriate thickness and resistivity of PSi layer for radio frequency applications. The porous silicon film obtained on Si wafers (PSi-S) with a resistivity of (1-10 Ω.cm) presented interesting results, especially for a PSi thickness 50µm where the porosity is around 65% with a high insulating surface area, a surface roughness less than 1 nm and a hardness value (≈1GPa). These values should be advantageous with regard to withstand different devices on top of PSi. The low cost of realisation of porous silicon starting by standard cheaper wafers, there outstanding structural, chemical and nanomechanical properties results make porous silicon an interesting candidate for RFIC (Radio-Frequency Integrated Circuit) for microelectronics applications

Chapter 3

SUBSTRATES WIDE BAND CHARACTERIZATION FOR RF APPLICATIONS

3.1 Introduction

Information and Communication Technologies (ICTs), constitute an important factor of development and a driving force of the global economy and at the base of ICTs, they are electronic chip technologies. Nowadays, the digital economy (software, telecommunications, online services ...) represents the most dynamic sector of the world economy, and as a result, in most developed countries, its growth rate is double from that of classical economics. It now accounts for over 25% of global growth.

With the increasing demand in terms of bandwidth, and the increase of the quality of the services (the emergence of LTE Advanced, then 5G), the researchers and industrial plan to deploy radio communications in the band mm-wave, this band allows rates of data transfers of the order of the terabits/s. It is clear that 5G should deal with a lot of type of use that generation of previous radio technologies. These focused on the transport of voice and then voice and broadband data services. So, the 5G must offer not only these traditional services (in an improved way), but also new services such as the Internet of Things (*IoT*) or the Internet Tactile (industrial automation, transport systems, health ...) **[92]**.The substrates on which those devices (electronic chip) are manufactured play a major role in achieving that level of performance.

As it is motioned in the chapter 1, high resistivity substrates (HR-Si, HR-SOI) suffer from the existence of fixed oxide charges in the buried oxide (BOX) layer and in the passivation field oxide, which leads to the formation of a highly conductive layer of carriers at Si/SiO2 interface. This parasitic surface charge (PSC) can be avoided by introducing a trap-rich layer between the HR-Si and SiO2 **[93]**. This alternative is either costly or process demanding. The introduction of porous silicon PSi as substrate is the best solution to overcome the entire problems encounter.

3.2 Transmission lines, microstrip and coplanar structures

Transmission lines (TL) are used to characterize the porous silicon substrate performances to check whether it is suitable for RF applications. The most common TL for RF characterizations are microstrip (MS) lines, coplanar strip lines (CPS) and coplanar waveguides (CPW). A graphical representation of these structures is shown in Fig. 3.1. Microstrip lines consist of a metallic strip deposited on top of an oxide on a PS substrate. The ground in this case is the metallic plate deposited on the opposite side of the silicon substrate.

In two other coplanar structures, the fabrication process differs only in the fact that the signal ground represents the other strip line or lines. These structures are being used in silicon technologies because of their low cost and easiness of fabrication. The important difference between MS on one side, and CPS and CPW on the other is the distribution of an electric field. In MS, the electric field is applied and concentrated along the whole substrate, between the two metallic plates. In this case, the field is perpendicular to the surface. On the other hand, in coplanar structures, the electric field is parallel to the substrate surface and is concentrated near the silicon surface. CPW structures are inherently particularly sensitive to variations of the electrical properties at the substrate interface, thus making them suitable to characterize the properties and analyzing the effect of parasitic conduction below the oxide. The penetration depth of the electric field for CPW structures depends on substrate resistivity, the slot width between the coplanar strips and signal frequency (Fig. 3.1).

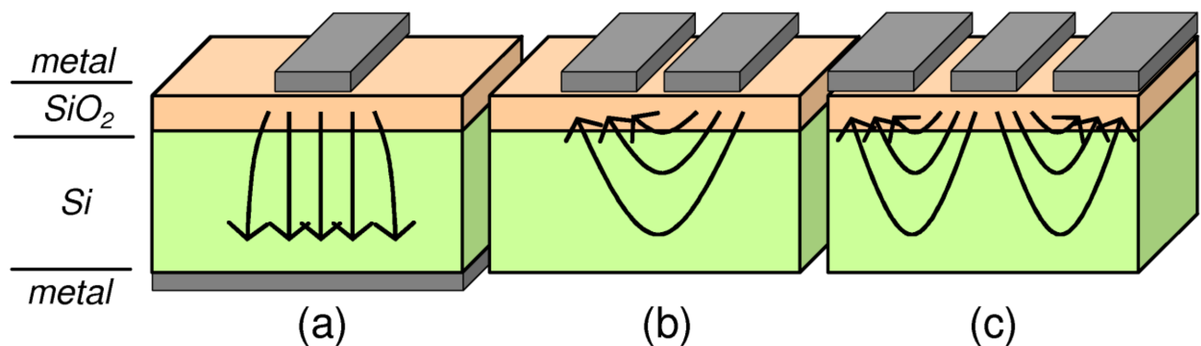


Figure 3.1 Schematic representation of (a) MIS microstrip line, (b) coplanar stripline and (c) coplanar waveguide and their electric field distribution **[29]**

Propagation modes

The propagation mode depends on the frequency of the applied signal and the substrate resistivity. Metal-insulator-semiconductor (MIS) transmission lines present three different operation modes lines: quasi-TEM, slow wave mode and skin effect mode **[94]**. These three modes are represented in Fig. 3.2 for both microstrip MS and coplanar waveguide CPW lines **[95]**.The skin-effect mode only appears extremely low-resistivity substrates are used, which is not the case for microwave and millimeter-wave applications.

Slow wave mode (lower-left region) occurs for moderate resistivity and frequency, the substrate acts as a semiconductor. In this mode conduction, currents dominate over the displacement currents and the propagated wave senses a larger capacitance than the two layer insulator semiconductor capacitance. Furthermore, there is a significant increase in the effective permittivity and reduction in wave velocity. This wave travels slowly **[94], [96]** and the magnetic field penetrates freely inside the substrate where The electric field is partly blocked. There is more interest in this mode as it is easily obtained, exhibits relatively low losses with large slowing factors and demonstrates little dispersion over a wide range of frequencies, it can be interesting for certain applications such as delay lines **[97]**...etc.

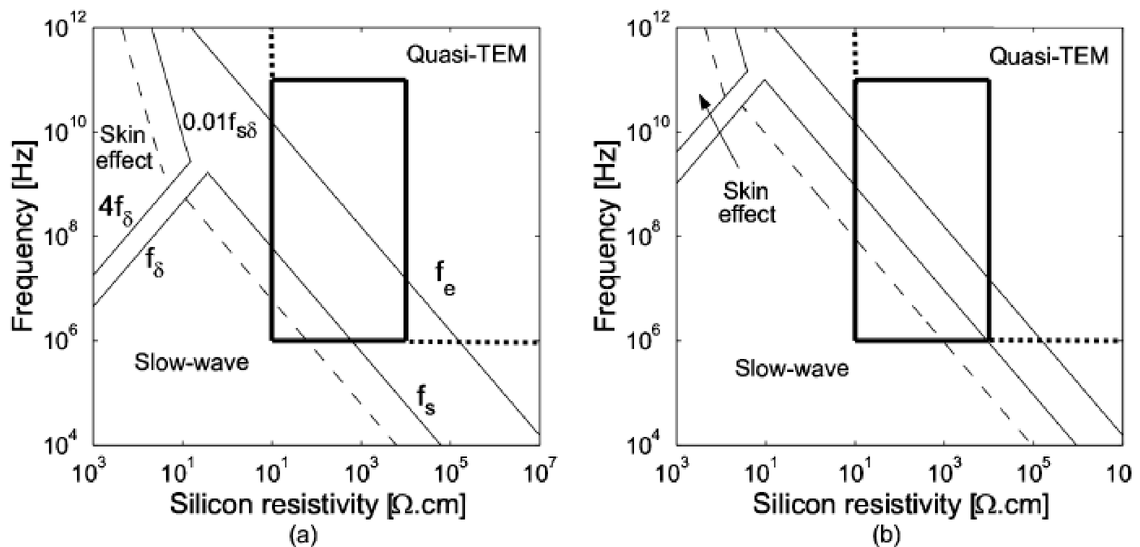


Figure 3.2 Resistivity vs. frequency domain chart for Si substrates of (a) MIS MS line and (b) CPW **[95]**

In the quasi-TEM mode, the insulator-semiconductor substrate behaves as a purely homogeneous dielectric. It appears when the product of frequency and the resistivity of the

substrate is large enough to produce a small loss tangent angle **[94]**. This occurs when the frequency (f) (Hz) is higher than the Si dielectric relaxation frequency (f_e) (Hz)**[95]**:

$$f = \frac{1}{2\pi\rho_{S_i}\,\varepsilon_{S_i}} \tag{3.1}$$

$$f_e = \frac{1}{2\pi}\frac{t_{ox}}{t_{sub}}\frac{1}{\rho_{S_iO_2}\,\varepsilon_{S_i}} \tag{3.2}$$

where$\varepsilon_{S_i}$is the dielectric permittivity of silicon (11.7 for silicon). In this mode, displacement currents dominate over conduction currents inside a substrate, thus the substrate behaves like a homogeneous lossless dielectric **[98]**.

The equivalent circuit is represented in Fig. 3.3 (a), where the series resistance (R_s) and inductance (L_s) are related to the metallic strip properties and the parallel conductance ($G_{sh} = G_{S_i}$) and capacitance ($C_{sh}^{-1} = C_{sh}^{-1} + C_{ox}^{-1} \approx C_{S_i}^{-1}$) to the substrate electrical properties.

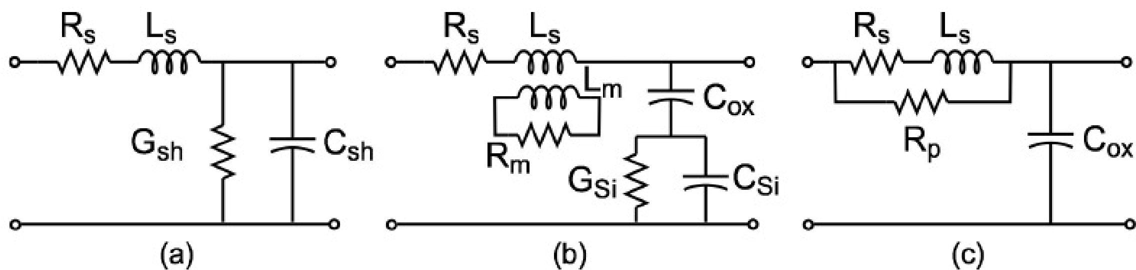


Figure 3.3 Equivalent circuit for (a) Quasi-TEM mode, (b) Skin effect mode and (c) Slow-wave propagation mode in MIS line **[95]**

For standard resistivity silicon substrates when operating at several GHz, propagationmodes are not clearly distinguished, as can be seen from Fig. 3.2. This region representshigh losses and is very dispersive according to **[95]** and the operating point liesbetween Quasi-TEM and slow-wave mode when interfacial polarization is still present.Porous silicon may be a good solution since the original substrate resistivity is (1-10 Ω.cm),but after the anodization process the effective resistivity may reach several kΩ.cm asshown later.

3.3 Characterization of CPW transmission lines

Using Maxwell's equations along with the constitutive relations between the electric and magnetic field and their corresponding flux densities the following can be inferred [10]:

$$D = \varepsilon E \tag{3.3}$$

$$B = \mu H \tag{3.4}$$

where$D$ is the displacement field and Hmagnetizing field. μandε are complex permeability and permittivity of the medium, respectively. Permeability is the measure of the degree of magnetization of a material in response to a magnetic field. Typically, Si broadly used in the semiconductor industry is considered as a non-magnetic material. Permittivity describes how much electric flux is generated per unit charge is induced in the material in the presence of an electric field. For the electrical polarization (P_e) of a dielectric material when an electric field is applied, Eq. 3.3 can be rewritten as:

$$D = \varepsilon_0 E + P_e = \varepsilon_0(1 + \chi_r)E \tag{3.5}$$

with

$$\varepsilon = \varepsilon_0(1 + \chi_r) = \varepsilon_0 \varepsilon_r \tag{3.6}$$

whereε_0 and ε_r are vacuum and relative permittivity respectively, and χ_r is the relativeelectric susceptibility. The imaginary part of the permittivity accounts for loss in the medium, and must be negative:

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' = \varepsilon_r' - j(\varepsilon_d + \frac{\sigma}{\varepsilon_0 \omega}) \tag{3.7}$$

whereε_d represents dielectric losses (heat generated due to vibration of dipoles) and σ represents conductivity losses. These terms are indistinguishable and are referred to as total effective conductivity loss. Further, the loss tangent can be defined as:

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} = tan\ \delta_d + \frac{\sigma}{\omega\varepsilon'} \approx \frac{\sigma}{\omega\varepsilon'} = \frac{1}{\rho\omega\varepsilon'} \tag{3.8}$$

where ε' and $\varepsilon''$are real and imaginary parts of complex permittivity, tan $\delta_d$is the loss tangent due to dipole relaxation, ω is the angular frequency and ρ is the electrical resistivity. tanδ_d can be approximated by the losses due to electrical conductivity (leakage losses) since substrate losses are higher than those caused by dipole relaxation. It is considered that a dielectric has low losses if tan δ< 0:1 (corresponding resistivity of ρ= 1.5 kΩ.cm at frequency of 1 GHz) **[29]**.

To calculate the attenuation constant, we start about the value of permittivity ε, which is not constant in all directions, and it can be expressed in form of matrices (tensors) for anisotropic materials. However, for a plane wave propagating in a free, isotropic and homogeneous conductor of any kind, a complex propagation constant can be defined for the medium that gives a relation between its electric and magnetic properties:

$$\gamma = \alpha + j\beta = j\omega\sqrt{\mu\varepsilon} \qquad (3.9)$$

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \qquad (3.10)$$

The real part,α is called the attenuation constant. It is the attenuation per meter of a signal that propagates through the medium and is expressed in nepers per meter (Np/m). The imaginary part, β is the phase constant which corresponds to the phase change per meter of propagated signal (rad/m). Considering a medium without magnetic losses, the expressions of α and βcan be obtained:

$$\alpha = \frac{\omega}{\sqrt{\varepsilon_0\mu_0}}\sqrt{\frac{\mu_r'\varepsilon_r'}{2}\left(-1 + \sqrt{1 + (\frac{\sigma}{\omega\varepsilon_r'})^2}\right)} \qquad (3.11)$$

$$\beta = \frac{\omega}{\sqrt{\varepsilon_0\mu_0}}\sqrt{\frac{\mu_r'\varepsilon_r'}{2}\left(1 + \sqrt{1 + (\frac{\sigma}{\omega\varepsilon_r'})^2}\right)} \qquad (3.12)$$

As the Si substrate used in industry can be consider non-magnetic material (μ_r = 1). Thus, if the propagation in the medium is known, the electrical properties of the material can

be extracted. If the loss tangent is close to zero ($\tan\delta = \frac{\sigma}{\omega\varepsilon_r'} \leq 0.05$), both equations (3.11) and (3.12) can be rewritten as follows:

$$\alpha = \frac{\sigma}{\sqrt{\varepsilon_0\mu_0}}\sqrt{\frac{1}{2\varepsilon_r'}} = \frac{\omega}{\sqrt{\varepsilon_0\mu_0}}\sqrt{\frac{\varepsilon_r'}{2}}\, tan\delta \qquad (3.13)$$

$$\beta = \frac{\omega}{\sqrt{\varepsilon_0\mu_0}}\sqrt{\varepsilon_r'} \qquad (3.14)$$

3.3.1 Transmission line model of a CPW

In the specific case of transmission lines for which transverse electromagnetic (TEM) waves are supported, Maxwell's equations can be reduced to well-known Telegrapher's equations developed by O. Heaviside **[99]**. In MIS structures, the transverse component of the electric field is significantly larger than the longitudinal component. The length of transmission lines are comparable to the wavelength of microwave signals. In a distributed-parameter network, currents and voltages can vary in phase and magnitude over the transmission line length. Telegrapher's equations model the transmission line as an infinite series of two-port elementary components of length Δz as shown in Fig. 3.4 **[100].** The lumped-element circuit consists of four circuit elements: series resistance R, inductance L, shunt conductance G and capacitance C, where all parameters are expressed per unit length.

The series inductance represents self-inductance of the two adjacent conductors in a transmission line, and C is the shunt capacitance between them. R represents losses due to conductivity of metal conductors, and G represents the dielectric loss around the conductors.

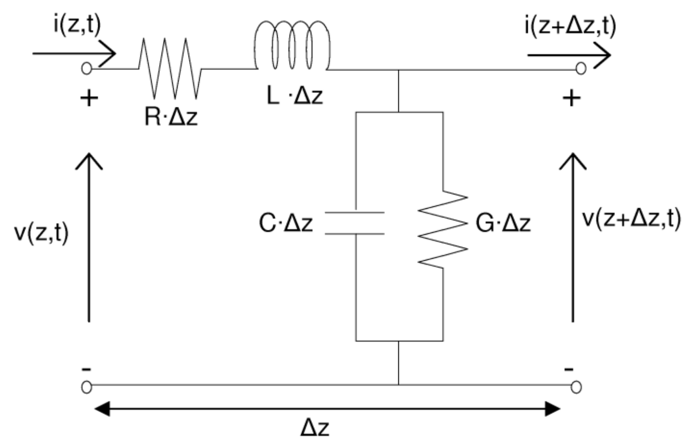


Figure 3.4 Equivalent circuit of a lumped-element model of a transmission line**[29]**

The Solving of the differential Telegrapher's equation **[101]** give the wave solution exponential form as follow:

$$V(z) = V_{in}e^{-\gamma z} + V_{out}e^{\gamma z} \tag{3.15}$$

$$I(z) = I_{in}e^{-\gamma z} + I_{out}e^{\gamma z} \tag{3.16}$$

From Eqs3.10, 3.15 and 3.16 the characteristic impedance of the transmission line, Z_c, is defined as the ratio between the voltage and current from the time-domain of the differential telegraph equations for a sinusoidal steady-state condition **[102]**:

$$Z_c = \frac{V_{out}}{i_{out}} = \frac{V_{in}}{i_{in}} = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \tag{3.17}$$

The R, L, G and C model parameters can be extracted from Eqs3.10 and 3.17:

$$R = \Re(\gamma Z_c) \tag{3.18}$$

$$L = \frac{\Im(\gamma Z_c)}{\omega} \tag{3.19}$$

$$G = \Re\left(\frac{\gamma}{Z_c}\right) \tag{3.20}$$

$$C = \frac{\Im\left(\frac{\gamma}{Z_c}\right)}{\omega} \tag{3.21}$$

At high frequency approximation, (i.e when $\omega L \gg R$ and $\omega C \gg G$), the total losses seen by the transmission line are described by:

$$\alpha_{tot} = \alpha_{con} + \alpha_{sub} \approx \frac{R}{2}\sqrt{\frac{C}{L}} + \frac{G}{2}\sqrt{\frac{L}{C}} \approx \frac{R}{2Z_c} + \frac{G}{2}Z_c \tag{3.22}$$

Where α_{con}areconductor losses (due to the resistivity of the metal) and α_{sub} are substrate losses (due to the coupling between the line and the substrate). The propagation constant is provided from the de-embedded measured S-parameters of the CPW line, whereas the characteristic impedance is extracted based on Dehan method **[103]**.

At high frequencies, the attenuation is a function of the square of the frequency due to the skin-effect **[104-105]**. The extracted relative permittivity diverges strongly at low frequencies due to the influence of RG product and at high frequencies, it converges towards a certain value. The CPW lines are not surrounded by isotropic and homogeneous material, that completely surrounds the line as the one shown in Fig. 3.5a, but with air as a top material, thus the permittivity that CPW line "sees" is the permittivity of its entire surrounding (Fig. 3.5b) Moreover, in the presence of fixed oxide charges and a layer of PSi, the substrate is not considered as homogeneous and it does not have a constant resistivity along its depth (Fig. 3.5c). The extracted values of resitivity (conductivity) and permittivity are the effective parameters of the line and not those of the silicon handle substrate. The above equation is thus corresponding to the equivalent homogeneous substrate as shown in Fig 3.5.

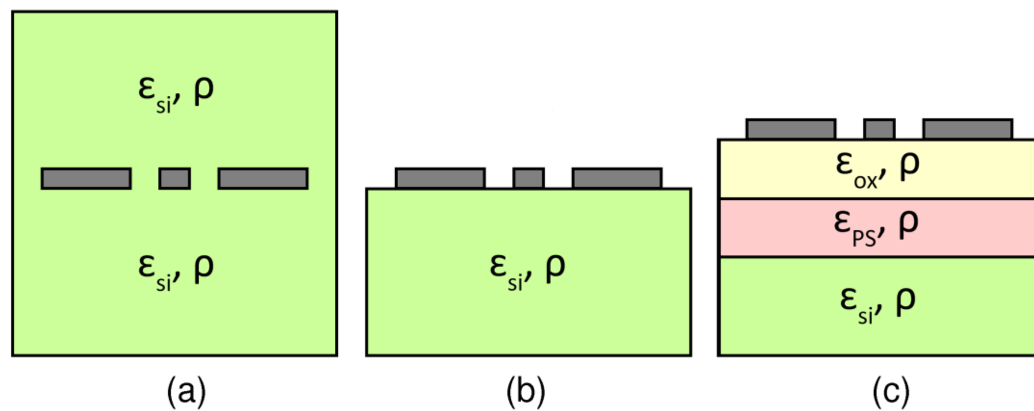


Figure 3.5 CPW line (a) in a homogeneous material, (b) on top of a homogeneous material and (c) on top of a non-homogeneous material resistivity **[29]**

3.3.2 Scattering parameters

The characterization of a simple 2-port linear network (Fig. 3.6) provides an easy way to describe the properties of a complicated network. When an RF signal is incident at one port, some fraction of the signal will bounce back out of that port, some of it will scatter and propagate to other ports, and a portion of it will disappear as heat or electromagnetic radiation. The relation between the incident and the reflected power waves are expressed using the scattering matrix or S-matrix. S-parameters **[106]** describe the network behaviour at a certain frequency, they refer to the scattering matrix, which is a mathematical construct quantifying how RF energy propagates through a multi-port network. The S-matrix for an N-port network contains N^2 coefficients (S-parameters), each one representing a possible input-

output path. These S-parameters are vectors, they have a magnitude and an angle, having both of this properties of the input signal changed by the network.

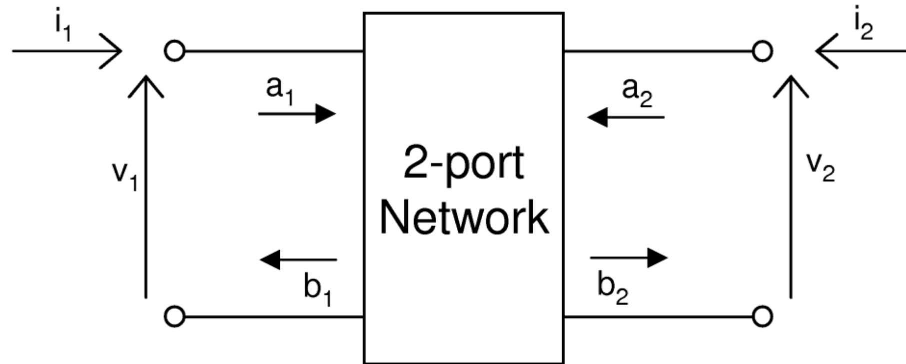


Figure 3.6 Schematic view of a 2-port network **[29]**

The S-parameter matrix,for a 2-port network has the following form:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{3.23}$$

The element (and its subscript) of the matrix, named Sij refer to the ratio of input signal from port j to the output port i. The diagonal elements are called reflected coefficients since they describe the reflected signal from a port, while off-diagonal elements represent transmission coefficients because they refer to two different ports **[29]**. For the behaviour of a simple 2-port network at microwave frequencies it is easier to quantify an amount of power or energy that goes in or comes out from each port than measuring the current and voltage at each port. The total amount of net power is equal to the difference between the incident powerfrom the source and the reflected power at the DUT input **[106].**

$$P = |a_1|^2 - |b_1|^2 \tag{3.24}$$

The a_1 and $b_1$are the incident and reflected power of waves at port 1, respectively. They are expressed in dB with a phase in radians. For a reference impedance of 50Ω the power of the wave can be written as **[107]**:

$$a_1 = \frac{v_1+50i_1}{2\sqrt{50}} \tag{3.25}$$

$$b_1 = \frac{v_1- 50i_1}{2\sqrt{50}} \tag{3.26}$$

$$a_2 = \frac{v_2+50i_1}{2\sqrt{50}} \tag{3.27}$$

$$b_2 = \frac{v_2-50i_1}{2\sqrt{50}} \tag{3.28}$$

The vector network analyzer (VNA) is the most frequently used measurement systems for characterizing microwave, passive or active devices. This system allow broadband analysis, typically from 10 MHz to the 100 GHz and it is used to measure the amplitude and the phase for each element of the S-matrix in Eq. 3.29.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.29}$$

Since the invention of the S-matrix which presents certain properties that allow can be easily characterized more complex circuits, engineers have developed design techniques, graphical representations and figures of merit (FoM) for different RF devices and circuits using S-parameters measurements. The use of the term ”scattering parameters” despite that the expressions found in this work correspond to pseudo-scattering parameters. A detailed explanation about the differences can be found in **[107]**.

Each element of the matrix can be calculated when the opposite port is shorted for a given value of the incident wave, thus each S element of the S-matrix can be calculated using **[108]**:

$$S_{11} = \frac{b_1}{a_1}, \text{ when } a_2 = 0 \tag{3.30}$$

$$S_{21} = \frac{b_2}{a_1}, \text{ when } a_2 = 0 \tag{3.31}$$

$$S_{22} = \frac{b_2}{a_2}, \text{ when } a_1 = 0 \tag{3.32}$$

$$S_{12} = \frac{b_1}{a_2}, \text{ when } a_1 = 0 \tag{3.33}$$

To investigate how efficiently porous silicon (PSi) provides RF isolation, the losses at high frequencies have estimated for CPW lines using power lossesor insertion losses **[18]**:

$$PL = 1 - |S_{11}|^2 - |S_{21}|^2 \tag{3.34}$$

Or

$$IL(dB) = -20 \cdot log|S_{21}| \tag{3.35}$$

As mentioned in the previous section, S-parameters are measured using a specific instrument named vector network analyzer (VNA). As shown in Fig. 3.7, VNA consists of a microwave source, series of detectors, attenuators, switches and 50 Ω matching loads. The S parameters at each port of the DUT are measured by connecting it at the VNA's test ports. One port is switched to a matched load when the other one is connected to the source.

The source generates a pure sinusoidal signal at a specific frequency at port 1. The detector R1 measure the delivered image of the incident wave after the first directional coupler by the source, thanks to the second directional coupler, the reflected wave is measured at detector A after the signal reaches the DUT. The measured signals are internally down converted and compared to the original source and to the phase reference using synchronous detection.

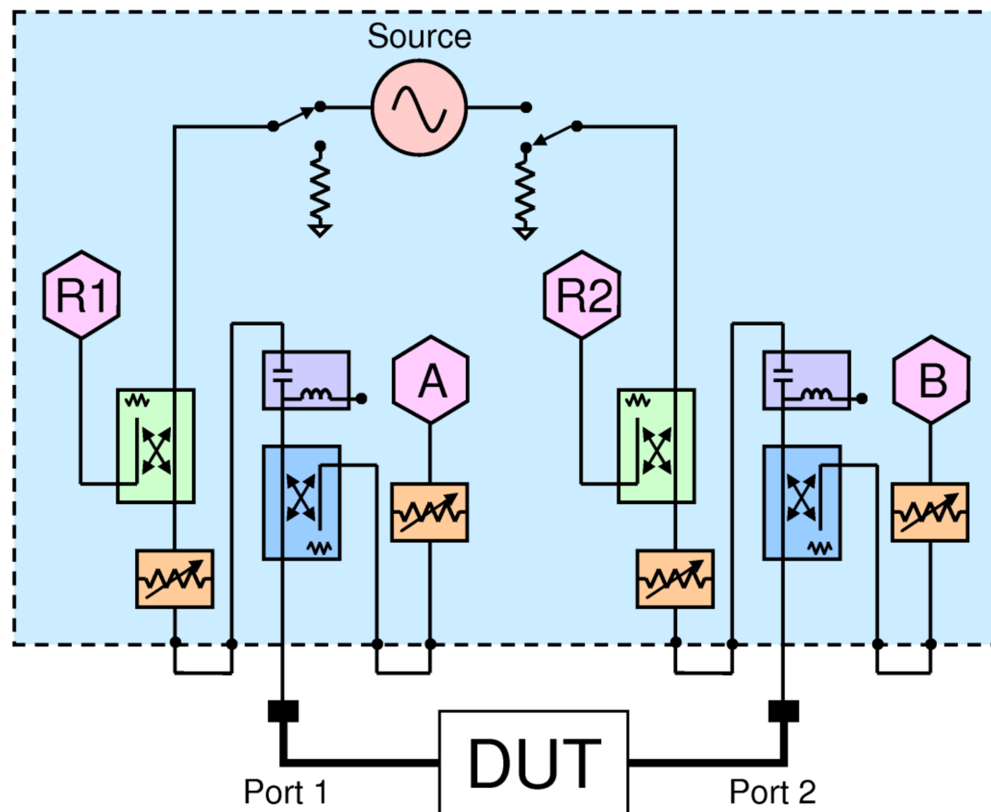


Figure 3.7 Schematic circuit of a 2-port vector network analyzer (AGILENT's PNA-X) **[109]**

Calibration is the process of characterizing the systematic errors of a VNA system. Once systematic errors are known and characterized, they are removed with a mathematical apparatus from raw measurements. Using this technique, VNA provides high accuracy of measurements. The calibration will move the reference planes of the measurement to the end of the test cables, it consists of calculating the error terms of the model chosen to describe the imperfections of the measuring system. For this, it is necessary to measure particular devices

called standards or calibration devices, fabricated on Impedance Standard Substrate (ISS), whose behavior is well known (Fig. 3.8). There are multiple methods developed for calibration. The used calibration techniques during these thesis work are SOLT(Short-Open-Load-Thru) and TRL(Thru-Reflection-Load). The SOLT calibration is the most common of all manual VNA calibration techniques. Figure 3.9 shows a simplified calibration substrate with short, open (open is performed by lifting the probe in air), line, and thru standards. It is a one-port measurement of each of the test ports using a known short, open and load termination. Following this the two test ports are connected to each other in a so called through connection. The pitch of the RF probe determines the dimensions of the RF pads of the CPW as shown in Fig. 3.10. It can be seen that the pitch is different from the slot width of the CPW, so the interface connection must be created between them. Unfortunately, these pads introduce parasitics and their effect must be removed to obtain the real S-parameters in a process called de-embedding.

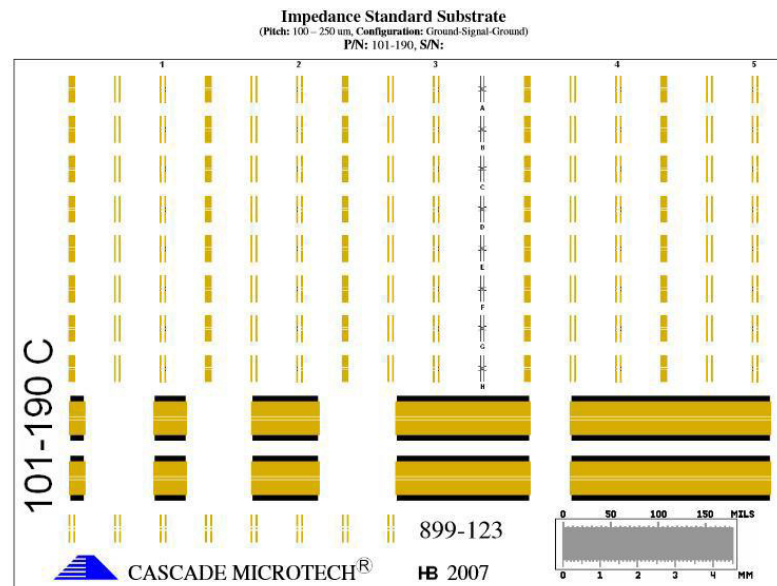


Figure 3.8 Standards fabricated on Impedance Standard Substrate (ISS) used for calibration

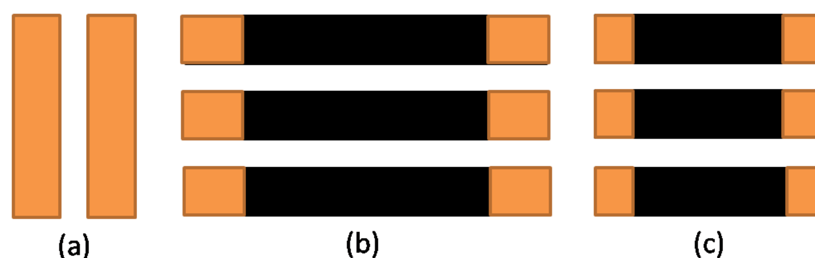


Figure 3.9 Layout of calibration standard for SOLT calibration: (a). short or open, (b) line, and (c). thru

The choice of method for de-embedding depends on the frequency, dimensions and shape of DUT (Device Under Test) and on the ability to control the standard's values. Between the different de-embedding techniques, TRL is used as a pad de-embedding technique **[103]**. After de-embedding, the reference planes are moved to the tips of theprobe.When the S-matrix is de-embedded, its S_{11} and S_{22} values are equal to zero. Fromthere the attenuation can be obtained easily **[110]** and further, other parameters of interest like permittivity and resistivity. However, it is rare to find an ideal transmission line withcharacteristic impedance perfectly equal to the 50Ω impedance of VNA's test ports.

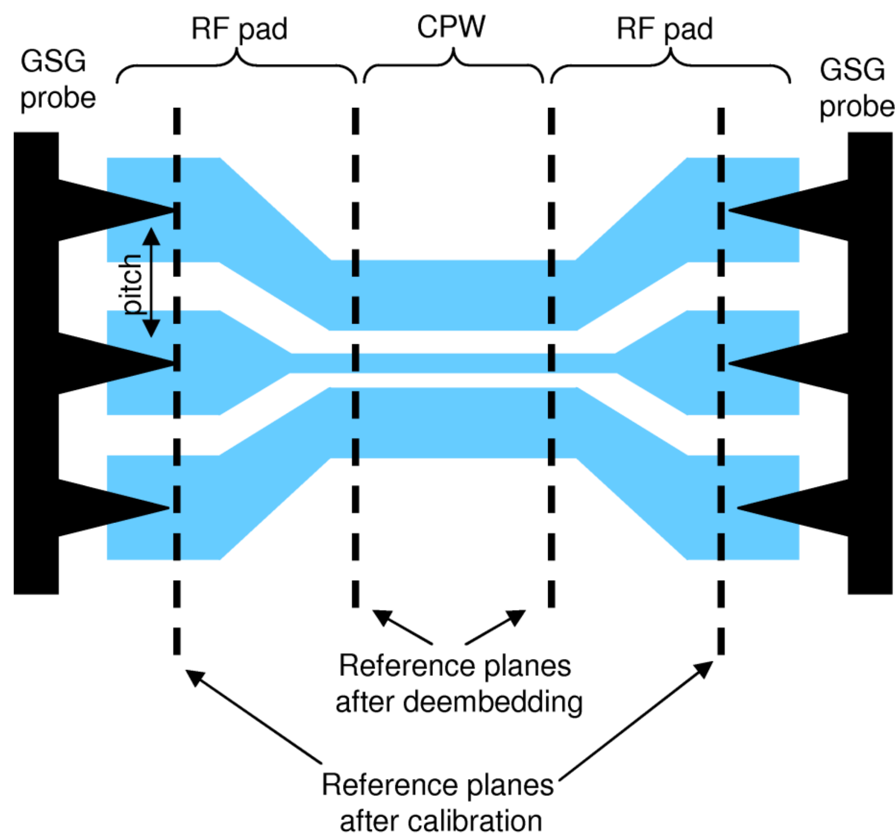


Figure 3.10 Reference plane before and after de-embedding **[29]**

3.3.3 Effective resistivity of a CPW transmission line

There are several material properties which have a major impact on the signal propagation, such as its electrical permittivity $= \varepsilon_0\varepsilon_r$, permeability $\mu = \mu_0\mu_r$, and the resistivity $\rho = \frac{1}{\sigma}$

Where ε_0 and μ_0 are the permittivity and vacuum permeability, respectively.

For a coplanar wave-guide fabricated on homogeneous dielectric with infinite thickness, the relative effective permittivity of the CPW line without conductor losses is given by:

$$\varepsilon_{reff} = \frac{C_{CPW}}{C_{air}} = 1 + q(\varepsilon_r - 1) \quad (3.36)$$

Where C_{CPW} and C_{air} are the lineic capacitances of the CPW on the investigated substrate and substituting it by air, respectively, and q a filing factor. The filling factor quantifies the difference degree between the capacitance of a CPW line when it is surrounded by air $(q = 0)$or using a dielectric substrate $(q = 1)$. In practice, the effective permittivity can be estimated to the value at which it converges at infinite frequency. If the CPW dimensions are known, and the following condition is maintained: h > 2(W + 2S), with h equal to the total substrate thickness **[102]**, the quality factor is approximated by 0.5 and the relative effective permittivity is directly calculated:

$$\varepsilon_{r\,eff} = \frac{(\varepsilon_r + 1)}{2} \quad (3.37)$$

Using Eqs. 3.18, 3.19, 3.20 and 3.21, once the characteristic impedance of the CPW line with the measured S-parameters are known the RLCG correspondent model is then denned and the substrate resistivity is be expressed by **[111]**

$$\rho_{sub} = \frac{1}{2}\frac{C_{air}}{\varepsilon_0}\frac{1}{G} \quad (3.38)$$

A new Figure of Merit (FoM) is proposed **[26]** of an approximated substrate as an homogeneous that have the same losses as the investigated nonhomogeneous, where the effective resistivity expression of substrate is given by:

$$\rho_{\mathrm{eff}} = \frac{1}{\sqrt{\varepsilon_{\mathrm{r\,eff}}}}\left(\frac{\varepsilon_{\mathrm{r\,eff}}-1}{\varepsilon_{\mathrm{r\,Si}}-1}\right)\frac{\sqrt{\mathrm{C_{air}}}}{\varepsilon_0}\frac{\sqrt{\mathrm{C_m}}}{\mathrm{G_m}} \quad (3.39)$$

With ε_{reff} is extracted using analytical formulas **[111].**

$$\varepsilon_{reff} = \frac{C_{CPW}}{C_{air}} \quad (4.39)$$

where C_m and G_m are the capacitance and conductance extracted from the measured propagation constant and characteristic impedance of the CPW line.

3.3.4 Measurement Setup of CPW characterization

All measurements presented in this thesis were made at the Wallonia Electronics and Communications Measurements (WELCOME) **[112]**.In order to make on-wafer measurement, the wafer is put on an on-wafer probe station (Fig.3.11) where mechanical arms allow connecting tips and RF probes to the device. The probes 150 µm |Z| GSG are connected to an Agilent N5242A PNA-X Microwave Network Analyzer using Süss™ through flexible coaxial cables and all the station is enclosed in a cage to prevent light coming in. RF impedance standard substrate (ISS) is used to calibrate the system with the port reference planes defined at the probe tips.

From the measured S-parameter, we extract the effective resistivity (ρ_{eff}), effective relative permittivity ($\varepsilon_{r,eff}$), RF line losses, and characteristic line impedance using the method described in **[26]**. A dedicated on-wafer short-open-line-thru (SOLT) calibration technique is used to remove parasitic components such as cables, connectors and other systematic errors. The calibration process aims at moving the measurement reference plane at the VNA to tips of the RF probes. A TRL (thru-Reflect-Line) de-embedding technique proposed by R. Gillon**[113]**is then used to remove unwanted parasitic introduced from the CPW RF pads and get the real S-parameters of the device under tests (DUTs), in a similar approach to a classical thru-reflect-line (TRL) de-embedding.

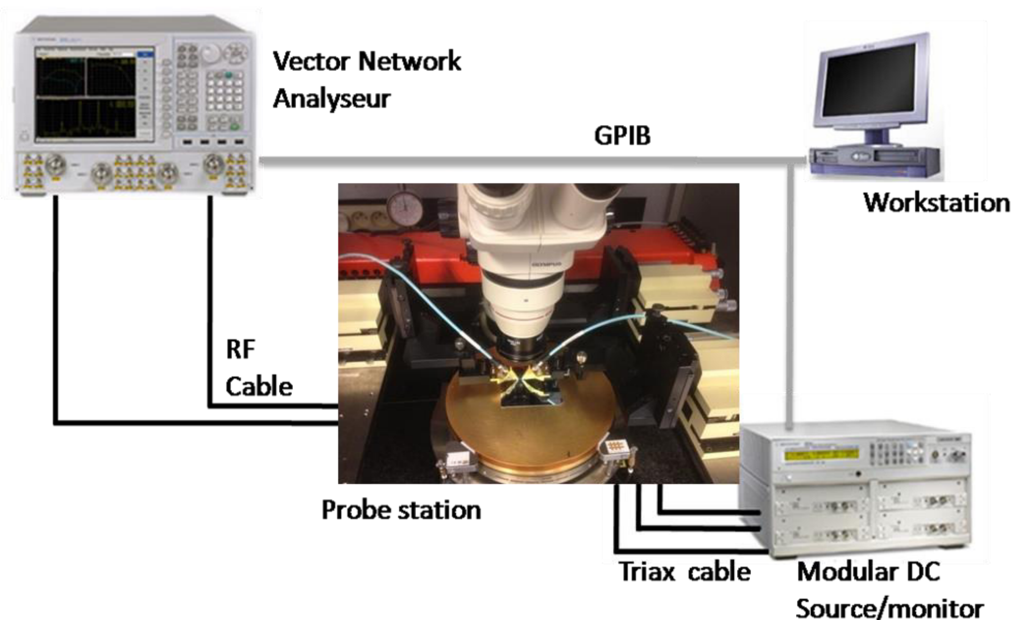


Figure 3.11 Introduction to On-Wafer Measurement at Microwave Frequencies

3.4 Harmonic distortion

For the characterization of passive components, small signals with a power not higherthan 0dBm is used, with the assumption that the device is operating in the linear region.A more accurate term would be “less non-linear”, because in practice all systems arenon-linear and introduce signal distortion. When the signal amplitude is large enough,the behaviour of an RF device varies with amplitude, and the operating region is notconsidered linear anymore. There are different techniques that can be used in order toinvestigate this non-linearity, and the technique used in this thesis uses the measurementof harmonics, mixing products and energy loss under large-signal operation. The figureof merit (FoM) for this non-linearity is total harmonic distortion (THD) and inter-modulationdistortion (IMD)**[114]**. This technique is well suited for the characterization of non-linearitiesin CPW lines on PSi.

3.4.1 Non-linear system

Considering a simple non-linear system, and a one-tone sinusoidal signal input, thefrequency spectrum will have two harmonic components added to the fundamental signalas shown in Fig. 3.12.

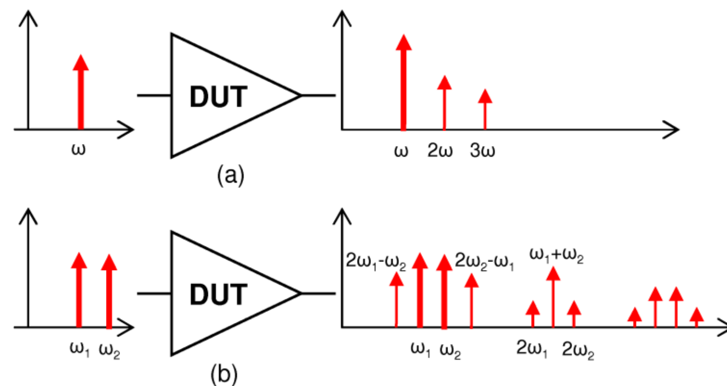


Figure 3.12 Frequency response of a non-linear system from (a) one-tone input and (b) two-tone input **[29]**

From energy conservation, it can be deduced that a part of energy is used to generate the harmonic components that distort (compress) the output signal. The integrated power of all the harmonics at the output is equal to the measured power at the fundamental (input). For non-linearities coming from the substrate, the THD can be approximated using 2nd harmonics **[29]**. A good way to characterize these non-linearities is to use CPW lines since they have a flat frequency response and lower attenuation **[29]**. As shown later, the harmonic

distortion (HD) is represented as a function of output power of the fundamental tone, and not the input power in order to avoid the false impression of harmonic reduction for substrates with lower effective resistivity and higher RF losses. Also, the 3rd harmonics represents the non-linearities due to metallic lines and contacts.

3.4.2 Setup for Harmonic Distortion characterization

The nonlinear characterization setup used in this work can be seen in Fig.3.13. It is based on a 4-port Agilent PNA-X vector network analyzer (VNA). A signal at 900 MHz and with power ranging from -25 to 15 dBm is generated by the internal source of the PNA-X and low-pass-filtered (LPF) to attenuate all its harmonics components below the measurement noise. The large-signal at 900 MHz is then injected into the CPW line placed on an on-wafer probe station and contacted through GSG RF probes provided by Cascade Microtech with a pitch of 150µm.ICCAP (Integrated Circuit Characterization and Analyses Program) is used for measurements, control, and data acquisition.

The output signal including the generated harmonics is filtered by a band-pass-filter (BPF) to remove the fundamental signal. The fundamental tone has enough power to generate harmonic distortion at the PNA detectors with higher power levels than the ones that we want to characterize. The first 4 harmonics components (H2, H3, H4 and H5) are detected at Port 4 using 4 different channels of the PNA-X. The external filters used in the setup impose the use of a fixed frequency for the fundamental tone of the large-signal. The frequency of 900 MHz was chosen since it corresponds to the fundamental frequency of the GSM standard.

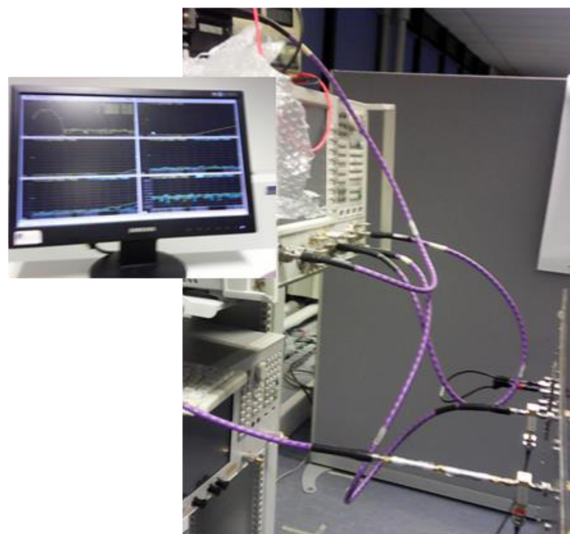


Fig. 3.13 Picture of the non-linear measurement setup

3.5 Integration of CPW lines on Si-based substrates

3.5.1 Si-based substrates preparation

3 inches wafers were processed at the Wallonia Infrastructure Nano FABrication (WINFAB) **[115]** facility at the Université catholique de Louvain, using standard clean room processes. Five types of substrates are fabricated and investigated in this study: standard p-type silicon Std (ρ = 1-10 Ωcm), high-resistivity silicon HR (ρ>4 kΩcm), trap-rich HR-Si (TR), and two porous Si substrates. Trap-rich HR-Si substrate consists of n-type HR-Si wafer with a nominal resistivity of 10 kΩ.cm, and a layer of 500 nm-thick trap-rich poly-Si deposited through low pressure chemical vapor deposition (LPCVD).The two porous Si substrates were fabricated, respectively, from standard p-type (100) silicon wafer(ρ = 1-10 Ω.cm, PSi-S) and highly doped p-type Si (ρ=5-20 mΩ.cm, PSi-M).

The porous Si substrates are annealed first in oxygen at 300°C for 2 hours to strengthen the microstructure, then under nitrogen at 420°C for 2 hours in order to stabilize the structure, the choice of the annealing parameters will be detailed in the next section. On top of the substrates, a 500 nm-thick silicon oxide (SiO_2) is deposited at 300°C by plasma-enhanced CVD, followed by 1 µm-thick layer of aluminum deposited by physical vapour deposition (PVD) for the definition of the RF CPW lines, the illustration of the five Si-based substrates is presented in Figure3.14.

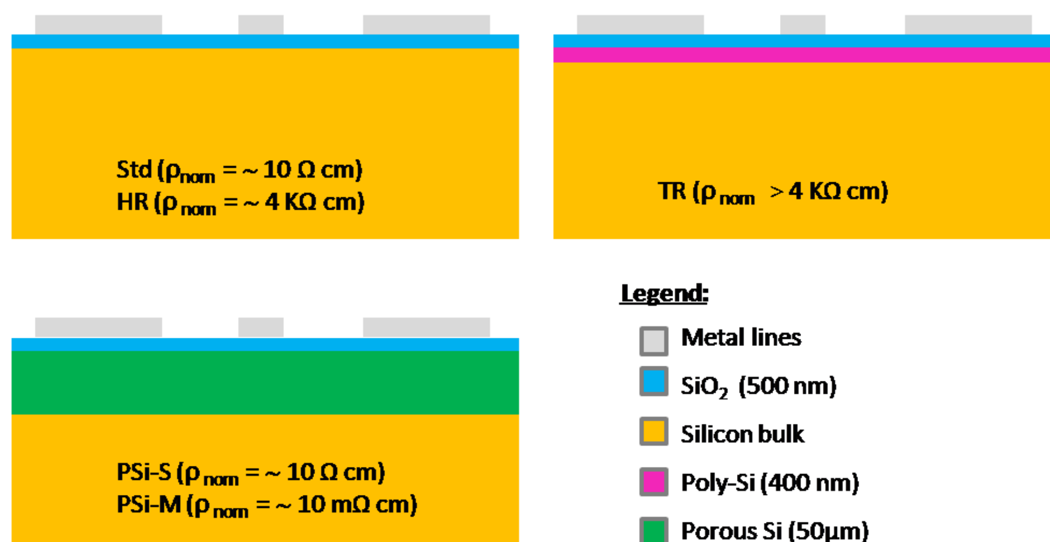


Figure 3.14 Illustration of the five Si-based substrates under consideration

3.5.2 Integration of CPW lines

Different lengths of CPW lines are fabricated on top of the oxidized substrates. The same CPW lines are integrated on the five above mentioned substrates, namely, Std, HR, TR, PSi-S and PSi-M. The dimensions of the CPW are: signal line width, W=38µm, signal line-to-ground plane distance, S = 18µm, ground plane width, Wg = 208 µm, and line length, L=8 mm, as sketched in Figure 3. 15.

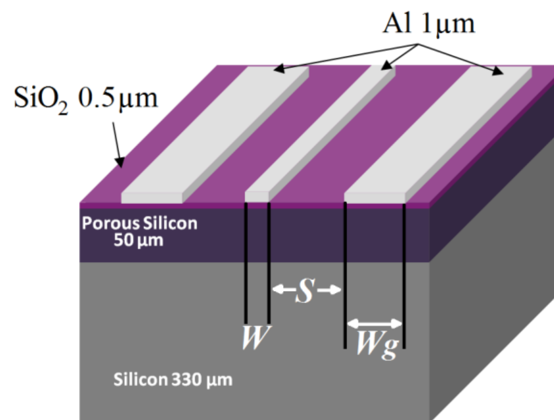


Figure 3. 15 Schematic of CPW transmission line fabricated on porous Si substrates

3.6 RF characterization of PSi substrates annealed at different temperatures

The fabrication of the structures on the wafers showed a poor adhesion of the structures as it is shown on the porous silicon substrates (Fig. 3.16). In order to have a better adhesion,the porous Si substrates are exposed to various thermal annealing conditions. The process described in the section 3.5 was applied on each substrate and a set of specific de-embedding structures is also included for an accurate extraction of device and substrate parameters.

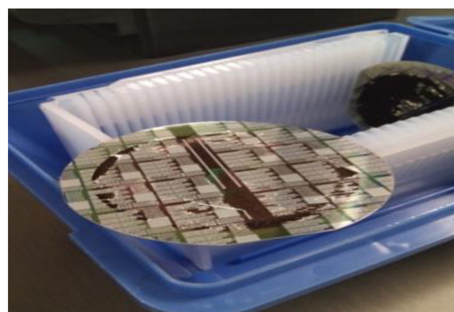


Figure 3.16 Picture of structures fabricated on porous silicon substrate

The thermal conditions for the five processes consist to expose the porous silicon substrate, in process A, to thermal oxidation at 300°C under dry atmosphere of O_2, in order to stabilize the whole structure mechanically for 1 hour, then at 800°C under N_2 for 1 hour, but before the thermal treatment, the Aluminum back-side was etched knowing that its melting point is 660°C. Process B0, the PSi substrates are annealed in nitrogen ambient at 300°C for 1 hour, followed by at 420°C for 1 hour, the same conditions are used for the process B1 except the Aluminum back-side of the PSi substrate was etched before the deposition of 500 nm PECVD oxide on top of porous silicon. For the process B2 the same thermal conditions than for the process B1 are used with different exposure time. Concerning the process B3, the material underwent through a thermal oxidation at 300°C under dry atmosphere of O_2 for 2hours, followed by annealing at 420°C for 2 hours in nitrogen ambient. Another process is used but not presented here, because the metallic lines did not adhere to the PSi substrate after a thermal treatment at 300°C under atmospheric pressure for 24 hours, the conditions of different processes used are described in Table 3.1.

Process	**Annealing temperature**	**Observation**
Process A	300°C(O_2)1h 800°C(N_2)1h	Etching Al-back side before thermal treatment
Process B0	300°C(N_2)1h 420°C(N_2)1h	//
Process B1	300°C(N_2)1h 420°C(N_2)1h	Etching Al-back side before PECVD
Process B2	300°C(N_2)3h 420°C(N_2)1h	Etching Al-back side before thermal treatment
Process B3	300°C(O_2)2h 420°C(N_2)2h	//

Table 3.1-Detailed description of process conditions

Influence of annealing temperature

So as to study the behavior of the PSi substrates according to the different processes summarized in Table 3.1, RF measurements of CPW lines are performed to extract the effective permittivity and resistivity of each substrate.

The effective dielectric permittivity extracted from the PSi substrates for five processes, is shown in Fig. 3.17 The lower value is found for the process B3, where in order to stabilize the whole structure mechanically, the wafer was exposed to thermal oxidation at

300°C under dry atmosphere of O_2 for two hours, followed by annealing at 420°C for 2 hours in nitrogen ambient. The combination between the thermal oxidation and annealing step under nitrogen gives the best results for the process B3. Fig.3.18 shows a good effective resistivity, in the case of process B3, which is much larger than those obtained by other processes.As shown in Fig. 3.19, the extracted $Z_c$value is stable towards the full measurement frequency range. Regarding the extracted attenuation presented in Fig. 3.20, the improvement can be appreciated at the process B3, where, after comparison, the attenuation decreases twice.

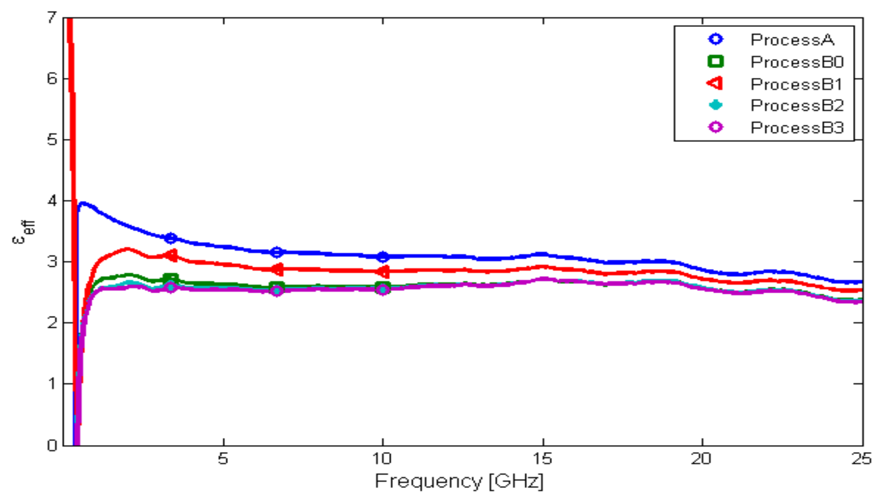


Figure 3.17 Effective dielectric permittivity (ε_{eff}) of CPW lines on5 different porous Si substrates

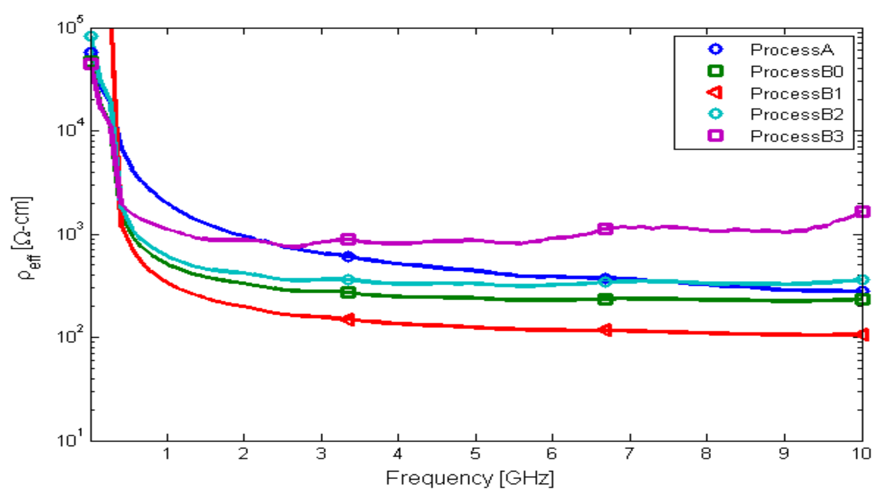


Figure 3.18 Effective resistivity (ρ_{eff}) of CPW lines on5 different porous Si substrates

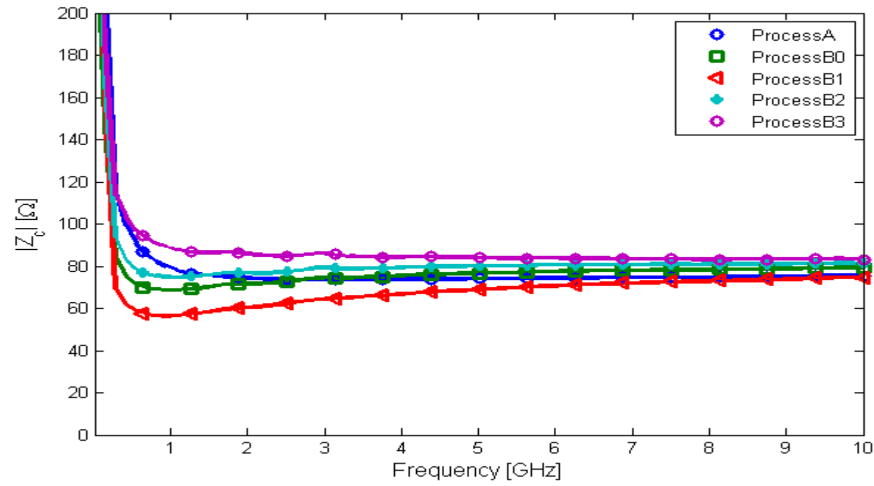


Figure 3.19 Characteristics impedance of CPW lines on5 different porous Si substrates

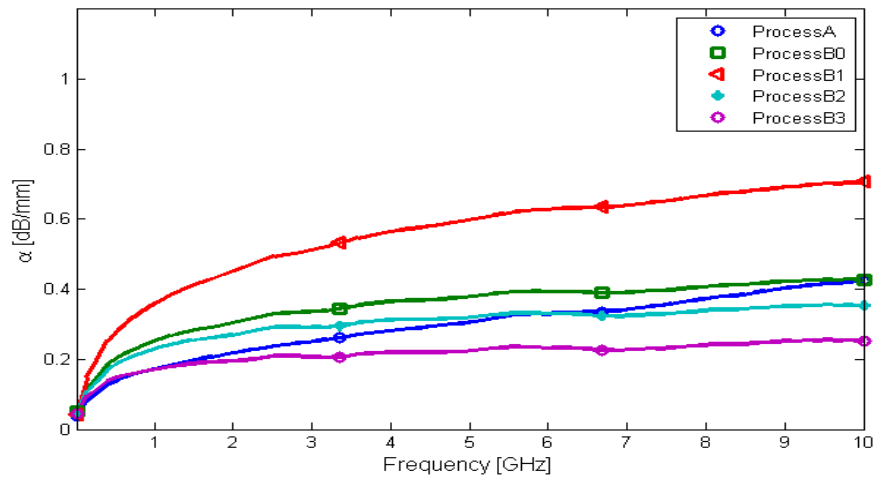


Figure 3.20 Attenuation of CPW lines on5 different porous Si substrates

From the experimental results, one can conclude that the process B3 is the best one for enhancing porous silicon substrate performances. After the manufacturing process, we see in Fig. 3.21 a good adhesion of structures on PSi substrates. According to the obtained results all experiments in this work have followed this same process B.

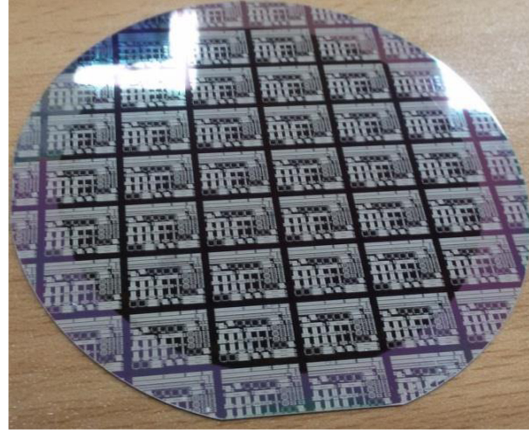


Figure 3.21 Picture of the wafer with the structures fabricated on PSi substrate with B3 annealing process.

3.7 RF characterization of Si-based substrates

3.7.1 Small-signal RF measurements of CPW

RF measurements of these transmission lines on the five substrates were conducted in the frequency range from 10 MHz to 26.5 GHz. From the method explained in **[103]**, the attenuation coefficient (α), the effective resistivity (ρ_{eff}), the characteristic impedance (Z_c)and the effective relative permittivity ($\varepsilon_{r,eff}$) are extracted from the CPW lines S-parameter measurements.And to confirm results the same measurement were carried out from 10 MHz to 67 GHz with an Agilent PNA-X vector network analyzer.

A comparison of the aforementioned extracted parameters is shownin Figure 3.22, 3.23, 3.24, 3.25. From Figure 3.22, The CPW lines on Std substrate present a low effective resistivity ρ_{eff} in the range of 10 Ω.cm. As a consequence, the RF losses of the lines are 3 dB/mm, see Fig. 3.23.

The HR substrate also shows poor performances effective resistivity ρ_{eff} and RF losses as for Std substrate. The lineic RF losses are around 1.4 dB/mm, which is a consequence of the value extracted from the effective resistivity (40 Ω.cm), and this is due to induced parasitic surface conduction (PSC) effects beneath the oxide layer that counterfeit the nominal high resistivity value of the silicon bulk **[116]**.

The addition of a thin poly-silicon layer, rich in traps, beneath the BOX and above a high nominal resistivity silicon bulk, eliminate the PSC effect **[7]**. These traps, capture the large amount of induced carriers present in the PSC layer, ensuring a state of strong depletion and high resistivity. The extraction of the effective resistivity from the CPW line measurements shows an increase of the ρ_{eff} of the order of 3 kΩ.cm and as a consequence, the RF line losses are at the low value of 0.35 dB/mm.

As we can see, the effective substrate parameters extracted from the CPW lines fabricated on PSi-M and PSi-S substrates exhibit excellent increased effective resistivities, around 7.7 kΩ.cm and 5.9 kΩ.cm, respectively. The RF losses of both PSi substrates are close to 0.18 dB/mm. By removing a large amount of the Si bulk material during the porosification process, the effective resistivity is increased due to the reduced conduction paths available through the substrate and due to the interface trapping states at the pore walls, which ensure a strong state of depletion similar to the trapping effects that occur in TR substrates.

Moreover, due to porosification, the extracted characteristic impedance Zc (Fig. 3.24), for the Std depicts 45 **Ω**, the HR and TR shows value around 50 **Ω**, however it is much higher for PSi-M and PSi-S, since they reached 70 **Ω** and 80 **Ω**, respectively. This larger value of Zc is due to their lower effective relative permittivities**[117]**. PSi-S and PSi-M exhibit low effective relative permittivities 3.5 and 5.5, respectively. As can be seen from Figure 3.25, thanks to these lower permitivitty, the crosstalk and noise coupling are reduced comparing to TR, Std and HR.

Finally the quality factor $Q = {}^{\beta}/_{2\alpha}$ of CPW lines obtained of the five substrates shows high values for PSi-S substrate (25.2 @ 26 GHz) and (58.3 @ 60 GHz), this make monolithic integration of RF components promising. Table 3.2 summarizes the characteristics of the investigated substrates.

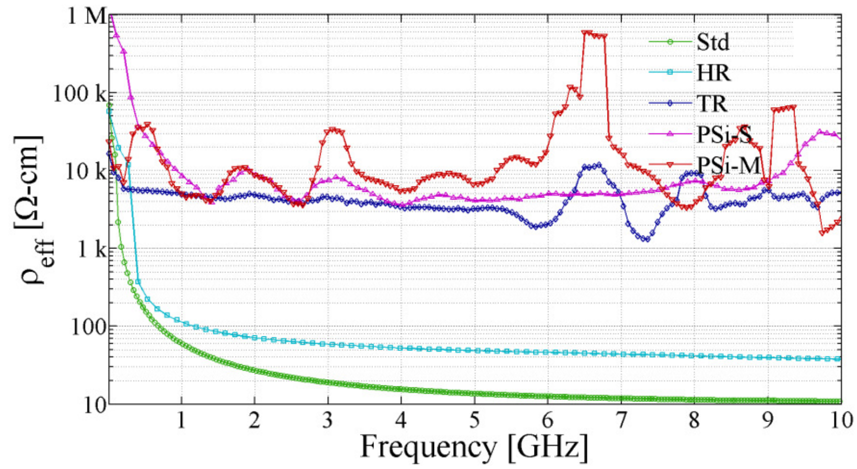


Figure 3.22 Effective resistivity of CPW lines lying on five different Si-based Si substrates

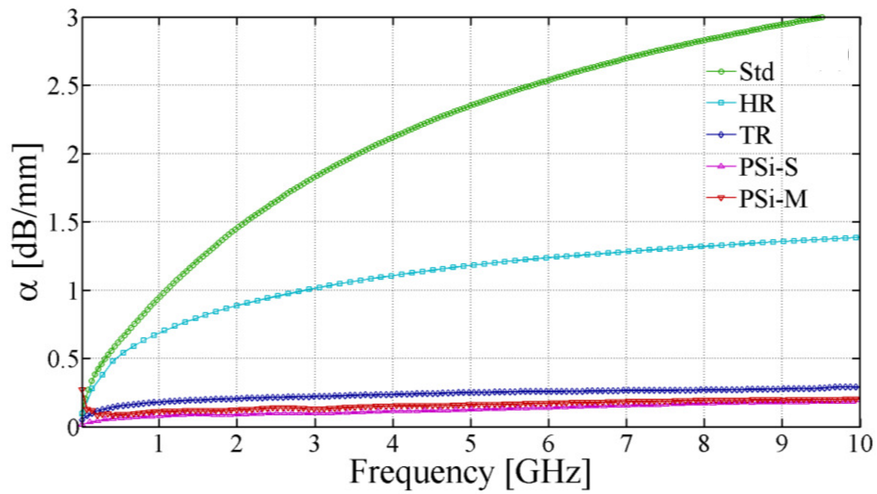


Figure 3.23 Attenuation of CPW lines lying on five different Si-based Si substrates

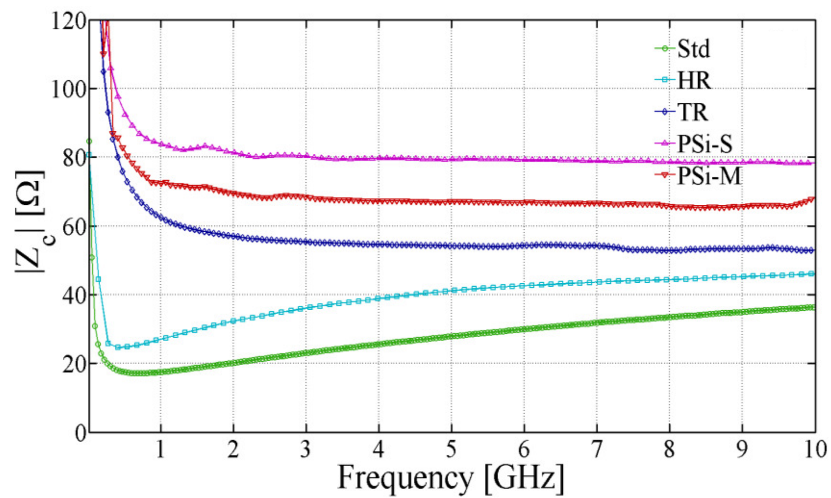


Figure 3.24 Characteristic impedance of CPW lines lying on five different Si-based Si substrates

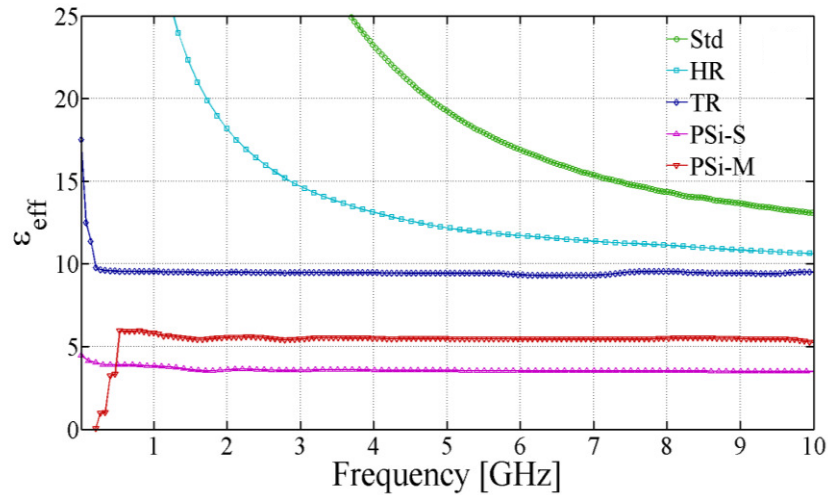


Figure 3.25 Effective relative permittivity of CPW lines lying on five different Si-based Si substrates

Substrates	Nominal resistivity (Ω-cm)	Porous thickness (μm)	Z_c	ε_{eff}	α (dB/mm)	Q@26/60GHz
Std	1 - 10	---	48	11.7	3.8	2.1/4.9
HR	> 4k	---	50	9.6	1.6	4.5/10.5
TR	> 10k	---	53	9.3	0.35	20.6/47.5
PSi-S	1 - 10	50	80	3.7	0.18	25.2/58.3
PSi-M	0.005 - 0.02	50	70	5.3	0.34	16.0/36.9

Table 3.2-Characteristics for Si-based substrates

3.7.2 Large-signal harmonic distortion of CPW lines

Large-signal measurements of the CPW lines were performed on-wafer using a dedicated setup **[6]** based on an Agilent 4-port PNA-X vector network analyzer. H2 and H3 components of the power at the output of the CPW on each substrate are plotted relative to the power of the fundamental component H1 in figure 3.26, at 900 MHz and the lines are biased to 0 V DC.

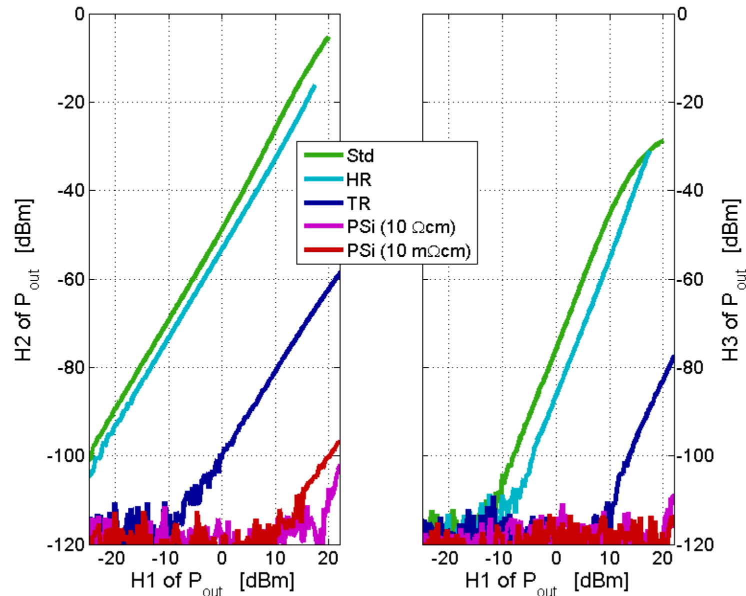


Figure 3.26 Comparison of the measured HD levels induced in 8 mm-long CPW lines implemented on the various Si-based substrates under consideration

The Std and HR substrates show high levels of harmonic distortion (HD). By introducing a poly-Si trap-rich layer beneath the BOX of a nominally HR substrate, reductions of more than 55 and 65 dB are obtained, respectively, for the second and third harmonics generated on a TR substrate. Interface traps and fixed charges at the Si-SiO_2 interface as well as substrate resistivity, significantly, influence the spatial charge distribution inside the Si substrate, and are therefore, expected to have a substantial impact of carriers on the substrate non-linear behavior, and it was proven that the distortion comes from the substrate itself and not from the metallic lines**[29], [118]**.

The harmonic distortion levels are further reduced when considering PSi as the substrate material. The second harmonic levels generated on PSi-S and PSi-M are, respectively, 34 dB and 46 dB lower than on TR. This increased linearity for PSiis explained by introduces trapping centers 50 µm-deep into the substrate volume, along the pore walls. In contrast of TR substrates, where traps are concentrated in a thin poly-Si layer.

3.8 Effect of temperature on RF performances

The co-integrate of complex digital circuits on the same chip with high performance RF analog and RF MEMS devices need to develop CMOS compatible substrate technology.

in addition, the development of wireless sensors operating in harsh environment for automotive, aerospace engine monitoring, monitoring electric machinery **[119-120]**. These systems will utilize efficient high power devices operating over 200°C.These systems will utilize efficient high power devices operating over 200°C. The maximum ambient temperature for the Si-based integrated circuits commercially available is about 85°C, which is sufficient for portable, communication and computing product applications. Military and automotive applications are typically rated to 125°C **[121]**.

In order to study the behaviour of Si-based substrates versus temperature, Small and large-signal high frequency measurements as function of high temperature ranging from 25°C up to 175°C on trap-rich HR-Si and porous Si substrates are compared with their corresponding initial HR-Si and standard-Si substrates, respectively. Using a probe-station endow by a Temptronics thermal 8-in chuck tool (Fig.3.27). Ground-signal-ground (GSG) (150 µm-pitch) high frequency Z probes are used for signal measurements.

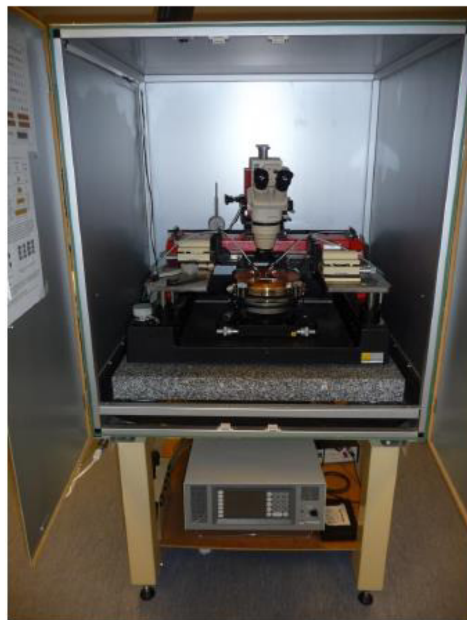


Figure 3. 27 On-wafer probing with Temptronics High Temperature control station

Before starting measurements, two calibrations steps are essential to extract the transmission lines parameters and to have fiable results. First, to set the measurement reference at the CPW probe tips, a SOLT (Short-open-load-thru) calibration technique is done using a standard calibration structures on an alumina substrate. Then, a TRL (Thru-reflect-

line) calibration is used to subtract the metallic CPW probe pad parasitics, and thus determine the characteristics of the designed CPW lines. The latter step is repeated for each temperature value. The achieved characteristics are shown in figures 3.28 and 3.29.

For both Std-Si and HR substrate in term of losses and effective resistivity, they are maintained over the whole temperature range. A gradual attenuation decrease on std-Si with temperature increase can be noted, this is equivalent to gradual increase of its effective resistivity due to a reduction in carrier mobility as temperature increases. The twofold increase in effective resistivity from 25°C to 175°C is in good agreement with the twofold decrease in carrier mobility given by Arora's models and measurements in **[122]**.

The HR's attenuation and effective resistivity varies little with temperature, they are practically stable. The negligible variations in the HR substrate, is that the coupling mechanism is through the parasitic surface conduction channel induced at the Si/SiO_2 interface **[123].**

Above 125°C the losses for both TR and PSi-M substrates depict small increase, this phenomenon is mainly due to the degradation of substrate resistivity with temperature, confirmed by the significant reduction of the extracted effective resistivity as is shown in (Fig. 3.28). This observation leads us to the hypothesis that the carrier concentrations in the porous layer of the PSi-M substrate drastically increase with temperature, thermally generated from the material's valence band.

On the other hand, the losses in PSi-S remain constant over the whole temperature range (Fig. 3.29), while, its effective resistivity, increase above 125°C, the reason is, as the size of the crystallites is too small, lower than 3 nm, so, the quantum confinement effect is observed, this effects confine the carrier energy levels to discrete states, rejecting the thermal generation of intrinsic carriers.

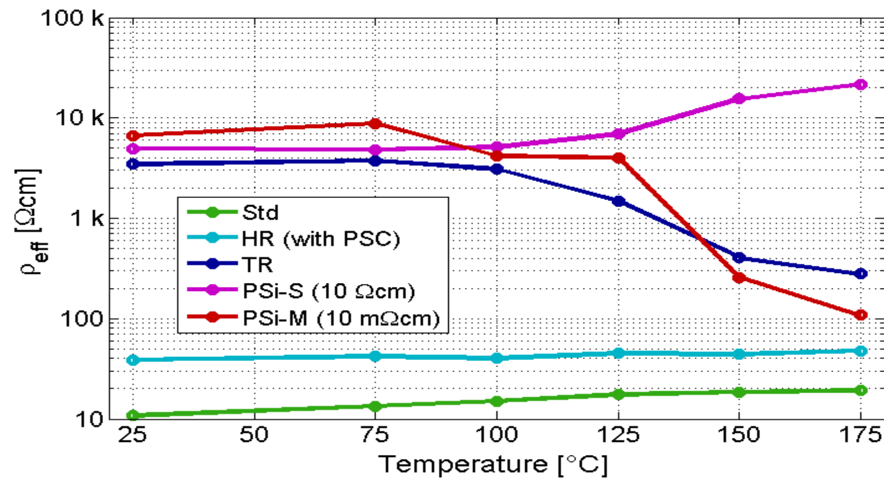


Figure 3.28 Effective resistivity extracted at different temperature points ranging from 25°C to 175°C for the five Si-based substrates

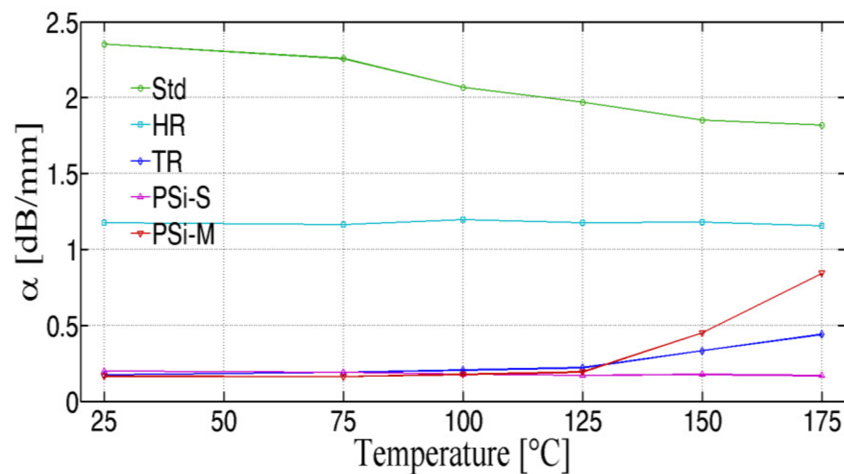


Figure 3.29 Losses extracted at different temperature points ranging from 25°C to 175°C for the five Si-based substrates

3.9 Conclusion

Finally, to figure out the interest of the reached insulating properties of the proposed substrate, the Table 3.3 summarizes our work **[124],** the comparison of PSi-S substrate versus pertinent works reported in the state-of-the-art. As it is observed through this table, the proposed PSi-S shows the highest quality factor which demonstrating thus the significant fall in parasitic related to the substrate.

	Techno	Line type	Freq(GHz)	ε_{eff}	ρ_{eff} (kΩ.cm)	α (dB/mm)	Q_{max}
This work	PSi-S	CPW	26	3.7	5	0.18	25
This work	PSi-S	CPW	60	3.7	5	0.18	58
[8]-1	PSi	CPW	100	2.2	NA	0.61	22
[8]-2	PSi	S-CPW	100	51	NA	4.4	15
[125]-1	BiCMOS-130-nm	μstrip	60	3.7	NA	0.5	20
[125]-2	BiCMOS 130-nm	S-CPW	60	13.3	NA	0.49	42
[126]	BiCMOS 130-nm ST	S-CPW	60	11	NA	NA	50
[127]	MNFM	SW-μstrip	60	36	NA	0.75	47

Table 3.3 Comparison of PSi-based transmission line performance to the state-of-the-art **[124]**

S-CPW: slow-wave coplanar waveguide

PSi: Porous Silicon

NA: Not Available

MNFM: Metallic-nanowire-filled-membrane

Chapter 4

ELABORATION OF A DEMONSTRATOR ON SI BASED SUBSTRATES

4.1 Introduction

Broadband systems are mainly the millimeterwave frequency band with its different applications reflecting the systems deployed in next-generation wireless networks.For eg, the 60 GHz frequency band has been the subject of several research projects for wireless network applications WPAN (Wireless Personal Area Network) [**128**-**129**]. Likewise, applications dedicated to vehicle radars are increasingly using the frequency band around 30 GHz.Similarly, the bands around the 28 GHz, 38 GHz and 73 GHz frequencies have been selected for the point-to-point or point-to-point links of the 5th generation (5G) of mobile telephony, which will be the future of telecommunications in the 2020s **[130-131]**.Thus, the millimeterwave frequency band ranging from 30 to 80 GHz is a major focus for wireless communication applications thanks to the wide frequency bands offered. These should allow a very important data transfer rate and a consequent miniaturization of circuit sizes, especially for passive structures such as bandpass filters.

The goal of demonstrator is to test the substrate performances through the integration of ademonstrator, this later, can to be, a filter, antenna, circulator or lines in mm-wave.

Why not a circulator? Because the fabrication process is very complicated, it summarized by a ferrite plate, a capacitor plus another ferrite plate and finally the encapsulation, we cannot manufacture it with the means that we disposal. Concerning the antenna, in literature, all the fabricated antennas are on PCB, for those reasons, we decided to design and manufacture filters.

In this chapter, the above-mentioned demonstrators circuit will be investigated and discussed through their broadband RF characterization.

4.2 Bandpass filter design in millimeter band

An in-depth study of the state of the art was conducted on the different contributions relating to the passband filter in the millimetric band during the last decade, we note that the presented works were realized on monolithic technologies and especially the CMOS technology in its different variants (0.18 µm, 0.13 µm, 0.35 µm ...) **[128], [130].** In addition, another very important observation was noted, is the fact that all filters consist of distributed elements.

Lan Nan et al **[132]** have used 0.18 µm CMOS technology, from a standard silicon substrate, six metal layers have been deposited as it is illustrated in Fig. 4.1. The band-pass filter was etched on the upper metal (M6) and the lower metal (M1) was chosen as the ground plane, the intermediate layers not being used. The obtained structure is similar to that of micro-ribbon technology, a conductor deposited on a dielectric (the five layers of SiO_2) with below a ground plane. Therefore, for the design of the millimetric bandpass filter that we will present in the next section, we will adopt this methodology considering that all the dielectric or semiconductor layers as being a substrate of equivalent electrical permittivity and of thickness which is the sum of the thicknesses of the different layers.

In order to evaluate the equivalent electrical permittivity and the equivalent thickness of the resulting substrate, we will use formulas (4.1) and (4.2) **[133]** respectively.

$$\mathcal{E}_{eq} = \left(\sum_{n=1}^{N} \frac{t_n}{\mathcal{E}_{rn}}\right)^{-1} . \left(\sum_{n=1}^{N} t_n\right) \quad (4.1)$$

$$t_{eq} = \sum_{n=1}^{N} t_n \quad (4.2)$$

Where ε_{rn} and t_n are respectively the electrical permittivity and the thickness of the nth layer of the process used.

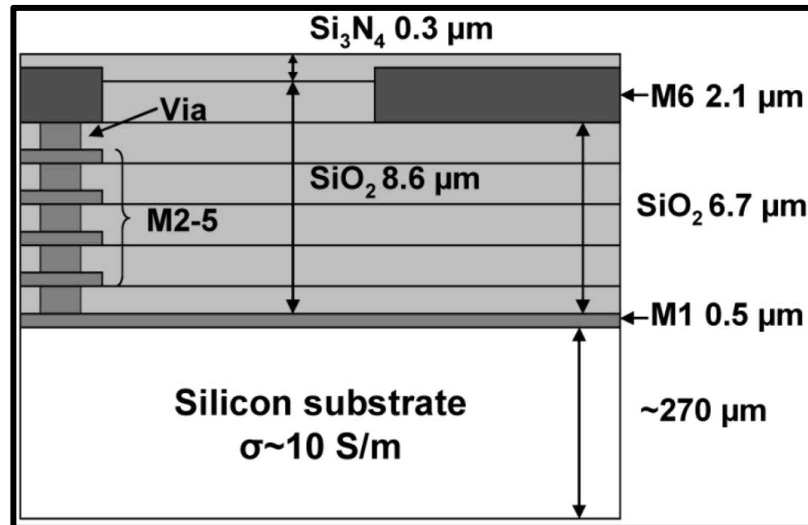


Figure 4.1 Layers constituting 0.18 µm CMOS technology

4.3 Electromagnetic simulation used in filter design

For the design of the millimetric bandpass filters, we will use the topologies by the coupled-line method discussed in **[134]**. The electrical parameters of the filter can be determined likewise the physical dimensions synthesized based on the values of the electrical permittivity and the equivalent thickness.The optimization of the final layout of the filter requires the use of electromagnetic CAD tools. In order to perform the different simulations, two methods were used. The first is to declare all the layers forming the process used, where each layer will be characterized by its own properties, namely its electrical permittivity, resistivity, tangential losses and its thickness. Figure 4.2 illustrates this method applied with the Momentum electromagnetic simulator of Keysight-ADS where the three layers constituting the process to use for etching the millimeter filter are well defined from, bottom to top: standard silicon, porous silicon and conductive layer.

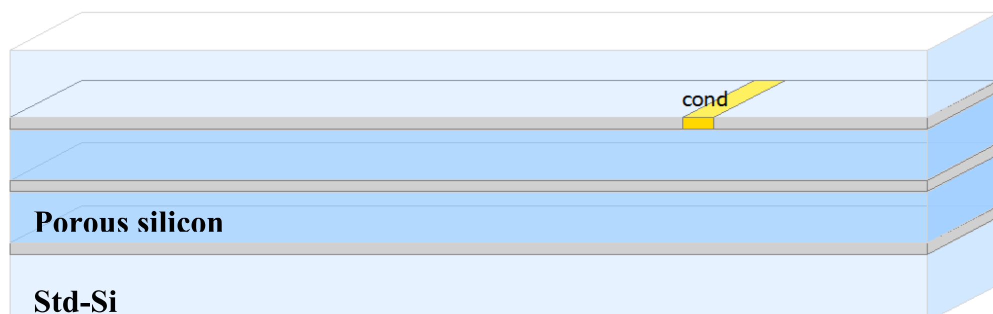


Figure 4.2 Simulation method No. 1 used in the design of millimetric filter

The second simulation method used consists of introducing a new material resulting from the different layers constituting the process used and whose equivalent physical properties are calculated from formulas (4.1) and (4.2). Figure 4.3 illustrates this second method applied with the Momentum simulator.

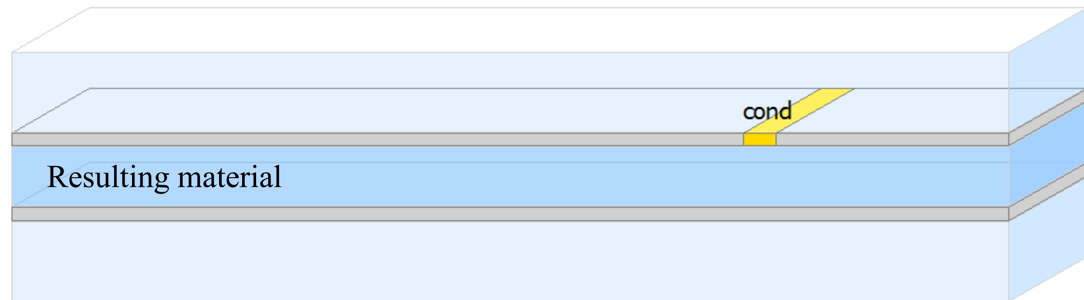


Figure 4.3. Simulation method No. 2 used in the design of millimetric filter

By observing the both figures relating to the two methods mentioned above, we can deduce that only one layer of metal was used. This leads us to design millimeter filter in coplanar CPW technology where the conductor and the ground plane will be supported on the same metal plane.

In reality, the choice of a CPW configuration is justified by two aspects. The first is related to the synthesis of the geometrical dimensions of the filter because the use of a microstrip topology forces us to place the mass plane below the standard silicon, in this case the ratios of the physical dimensions (width, substrate thickness, conductive thickness) do not give practical values. The second aspect, concerns the distribution of field lines; by retaining a CPW structure, only the porous silicon will be flooded by the field lines (provided of course to choose the appropriate thickness) whereas the standard silicon will be little affected; as a result, the filter will be able to fully benefit from the interesting characteristics of the porous material (low permittivity and high resistivity).

4.4 Millimetric filter on Si-based substrates

To validate its utility for millimetric passive circuits, the proposed PSi substrate is used to integrate millimeter-wave bandpass filters. The filter is designed around a frequency of 27 GHz that is suitable for the 5G wireless broadband communication involved in *IoT*. In order to design the band-pass filter on the proposed PSi, the resistivity and permittivity values extracted experimentally in section 3.7were considered.

The topology retained is an interdigital filter given by the direct-coupled method **[135]**. The figure. 5.4 schematizes the configuration of this filter which consists of a network of n quarter-wave resonators (possessing length $l_i$and width w_i) coupled to each other, through the interstices $S_{i,j}$. The filter is excited by two power supply lines 50 Ω with admittance Y_t, which are placed at a specified electrical length$\theta_t$to ensure impedance matching of the filter, this parameter could be evaluated by the equation4.3**[135]**,

$$\theta_t = \frac{\sin^{-1}\left[\sqrt{\frac{Y\, sin^2\,\theta}{Y_0\, g_0 g_1}}\right]}{1-\frac{FBW}{2}} \tag{4.3}$$

The parameters of equation (4.3) are defined as follows:

- FBW is the fractional bandwidth of the filter set at the center frequency of 27 GHz;

- $Y_0$is the reference admission;

- $g_0$and $g_1$are the normalized elements of the low-pass prototype, where the second-order Chebyshev function is involved in our design;

- θ and Y are expressed, respectively, by

$$\theta = \frac{\pi}{2}\left[1 - \frac{FBW}{2}\right] Y = \frac{Y_1}{\tan\theta} \tag{4.4}$$

The parameter $Y_1$is chosen so that the characteristic impedance of the supply line Z_t = 1 / $Y_t$be equal to 50 Ω**[135]**and knowing that $Y_t$is given by (4.5).

$$Y_t = Y_1 - \frac{Y_{1,2}^2}{Y_1} \tag{4.5}$$

Characteristic admittances $Y_{1,2}$ inverters J can be calculated from (4.6)

$$J_{i,i+1} = \frac{Y}{\sqrt{g_i\, g_{i+1}}} \quad i = 1, n-1$$

$$Y_{i,i+1} = J_{i,i+1}\sin\theta \quad i = 1, n-1 \tag{4.6}$$

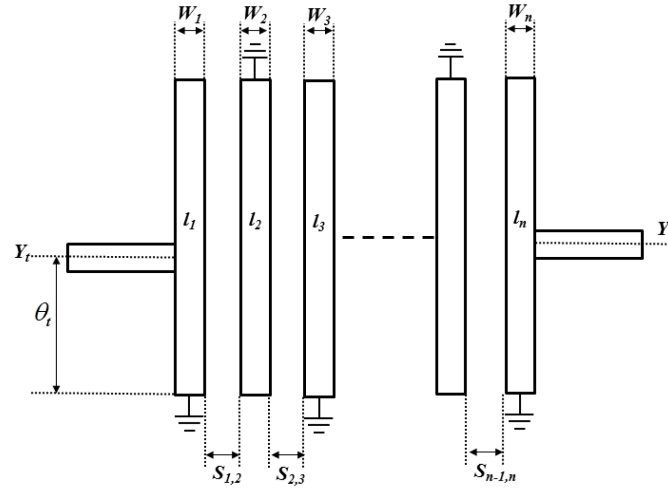


Figure. 4.4 General configuration of the interdigital band filter **[135]**

In addition, since the filter topology is based on a coupled line, the odd / even mode analysis is involved in filter design and the following formulation is used to evaluate the impedance of each line**[135]**:

$$Z_{e1,2} = \frac{1}{Y_1 - Y_{1,2}}, Z_{o1,2} = \frac{1}{Y_1 + Y_{1,2}}$$

$$Z_{ei,i+1} = \frac{1}{2Y_1 - 1/Z_{ei-1,i} - Y_{i,i+1} - Y_{i-1,i}} \qquad i = 2, n-2$$

$$Z_{ei,i+1} = \frac{1}{2Y_{i,i+1} + 1/Z_{ei,i+1}} \qquad i = 2, n-2 \tag{4.7}$$

$$Z_{en-1,n} = \frac{1}{Y_1 - Y_{n-1,n}}, \qquad Z_{on-1,n} = \frac{1}{Y_1 + Y_{n-1,n}}$$

Where$Z_{ei,\ j}$ and$Z_{oi,\ j}$ are, respectively, the odd and even mode impedances associated with the two considered lines$_i$and$_j$.

The layout and fabrication of the filter is depicted in figure 4.5, where a second order filter is synthesized in CPW configuration. It is important to note how the choice of CPW configuration is crucial. Unlike a microstrip structure, the CPW configuration keeps the filter near to the PSi layer (Fig.3.15 in section 3.5.2) enabling the full benefit from the PSi insulating properties. In addition, having the ground on the same face as the filter prevents the

use of vias, which can increase the losses coming from shunt resistances.

The filter response is adjusted by optimizingthe filter dimensions using the electromagnetic simulator Momentum of ADS 2015 (Keysight technologies).The structural parameters as defined in Fig. 5.5 (left) are (all in µm): *a*=15, *b*=3, *c*=67.5, *d*=75, *e*=30, *f*=100, L_1=963.5, L_2=263.5. The designed filter is integrated on all the investigated substrates depicted in Table 3.2 in section 3.7.1.

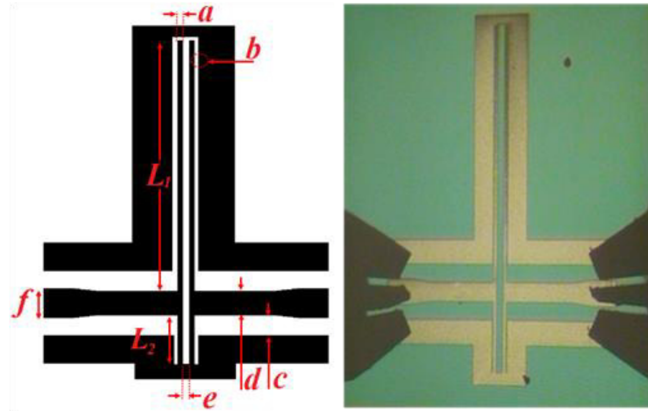


Figure. 4.5 Layout (left) and photography being measured on the probe station using 67 GHz GSG picoprobes (right) of mm-wave bandpass filter in CPW configuration

4.5 Characterization of the fabricated filter

The characterization of the fabricated filter is carried out from 10 MHz to 67 GHz with an Agilent PNA-X vector network analyzer. Before measurements, calibration and de-embedding techniques were performed by the SOLT method **[136].**

The measured data are plotted, against the simulated ones, and shown in figures4.6and 4.7. A good agreement between simulations and measurements is obtained, except for a widening in the bandwidth. The bandwidth widening is mainly due to a decrease in the capacitive Q factor of the bandpass filter. Such behaviouris expected as it might be related to the contamination of the silicon layer during the fabrication process. The utilized CAD tool conducts an electromagnetic (EM) simulation of the considered structure without accounting the effects of contamination tied to the manufacturing process. Therefore, the behaviour of the filter when integrated on the real physical substrate cannot be accurately predicted.

Nevertheless, it is evident from the measured performances that the insertion loss of the filter implemented in TR substrate returns with the best value with almost similar performance to PSi-S and PSi-M.

However, if we compare the measured responses of PSi-M and PSi-S, the latter depicts more interesting insertion loss with only 3.5 dB and remains constant over the operation band leading to a flat filter response, whereas, the former shows about 4 dB of losses which increase with frequency, thus, the filter flatness is lost. The filter flatness for the TR, PSi-S and PSi-M substrates is quantified, respectively, over the average insertion loss as follow: 2.82, 3.25 and 5 dB. These latter values are calculated by(max IL + min IL)/2.

Additionally, the frequency shift of the TR filter response is due to the value of its permittivity (ε_r =11.7) which is higher than the PSi permittivities (ε_r =3.5 and 5.5). Since, the filter was designed relying on the value of PSi permittivity, it was expected to obtain such a frequency shift in the trap-rich filter response (and the EM simulations highlight this behaviour).

Finally, PSi-S and TR are the most suitable substrates for designing mm-wave bandpass filters, nonetheless, if we consider the fabrication process, the realization of PSi-S is less complicated, consequently it offers low-cost alternative to trap-rich high-resistivity silicon.

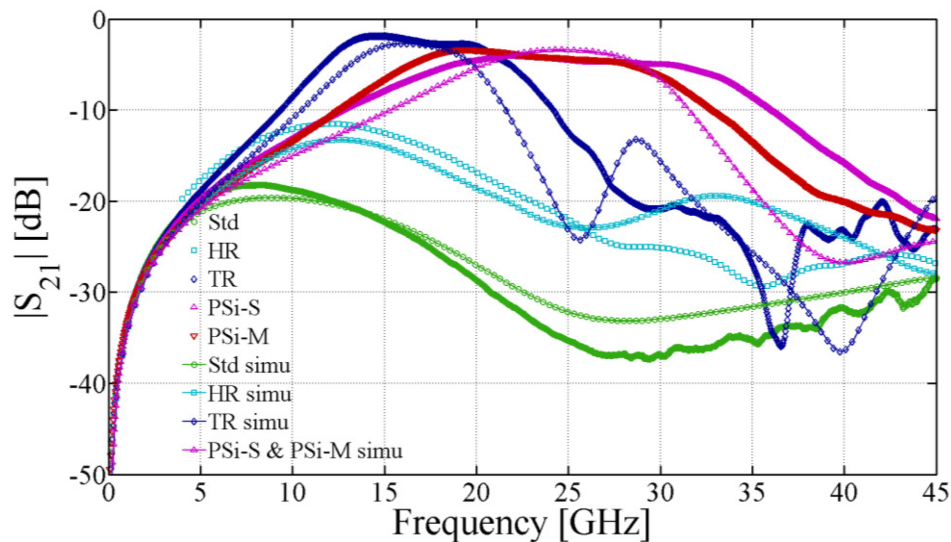


Figure 4.6 Insertion loss of mm-wave filter implemented
on various Si-based substrates

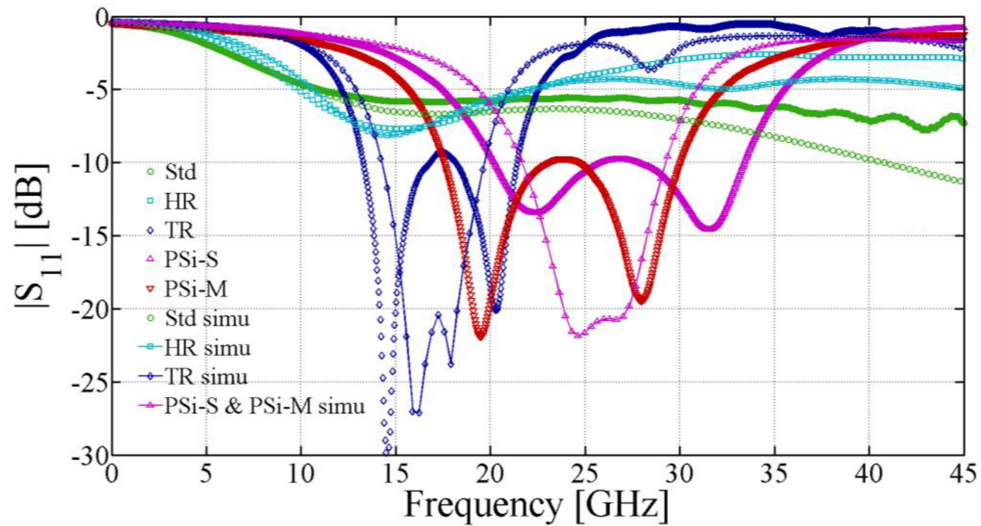


Figure 4.7 Return loss of mm-wave filter implemented
on various Si-based substrates

4.6 Effect of temperature on the RF performance of the bandpass filter

In this section, we are trying to evaluate the reliability of the proposed substrates against environmental parameters variation; in this case, the temperature variation is investigated. The filter integrated on PSi-M and PSi-S substrates is measured in air at 1atm and left around 1 h at various temperature points before carrying out S parameter measurements. As observed in figures4.8 and 4.9, the filter response remains almost unchanged even at high temperature. The values of the insertion loss at the different temperatures are summarized in Table 4.1.

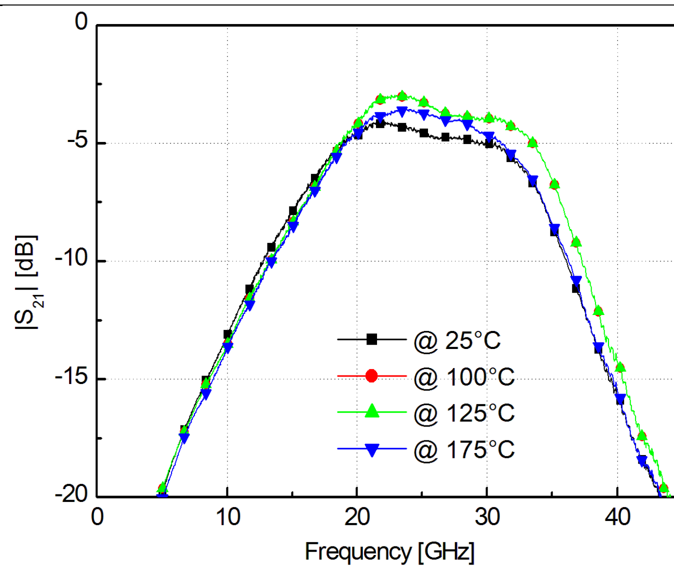


Figure 4.8 Mm-wave filter insertion loss at various temperatures on PSi-S substrate

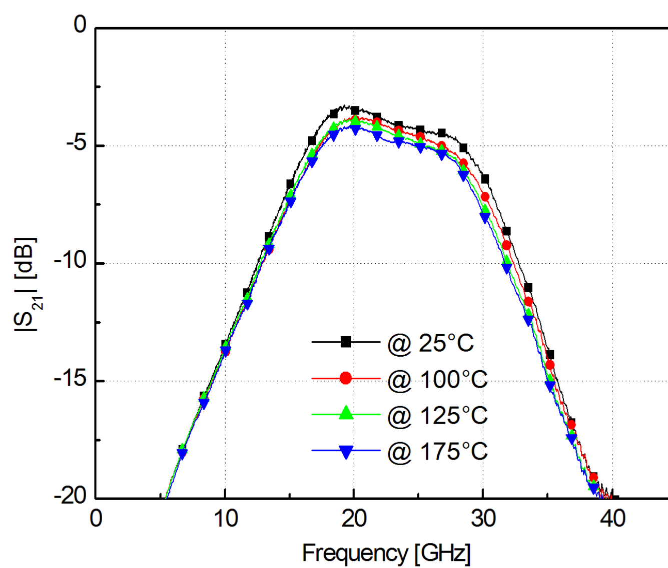


Figure 4.9 Mm-wave filter insertion loss at various temperatures on PSi-M substrate

Temperature (°C)	PSi-S $\lvert S_{21} \rvert$ (dB)	PSi-M $\lvert S_{21} \rvert$ (dB)
25	- 3.5	-4.5
100	- 3.6	-4.5
125	- 3.6	-4.8
175	- 3.9	-5.4

Table. 4. 1. Variation of the insertion losses with temperature

4.7 Results and discussion

Besides the conclusion made above regarding the preference of PSi-S versus TR, it is primacy of place to highlight the advantages of integrating mm-wave filters in PSi-S against their conventional integration in 0.18-µm CMOS technology or even the other CMOS technologies. Aiming to figure out this aspect, we have compared the performance of the PSi-S-based mm-wave filter to relevant works tied to mm-wave filters fabricated in various CMOS technologies, this comparison is summarized in Table 4.2.

	Central frequency (GHz)	Bandwidth (GHz)	Technology	Structure	Filter order	Size (mm^2)	Minimum IL (dB)	Maximum IL (dB)	$\|S_{11}\|$ (dB)
This work	27	14	PSi-S	Interdigital	2	1.36	**-3.5**	**-4**	**-13**
[137]	35	16	0.18-μm CMOS	FolddedInterdigital	2	0.12	-5	-7	-9
[138]	60	6	0.18-μm CMOS	Parallel coupled line	3	0.95	-10	-12	-11
[130]	51	7.5	0.18-μm CMOS	Thin film microstrip	3	1.10	-10	-11	-6
[139]-1	61.8	11.2	0.13-μm CMOS S-CPW	T-Junction	1	0.10	-2.2	-3.2	-12
[139]-1	60.8	10.1	0.13-μm CMOS S-CPW	T-Junction	2	0.29	-4.2	-4.8	-12
[140]	53.4	5.2	65-nm CMOS SWS	Rectangular open Loop	2	0.087	-5.5	-6.5	-13
[141]	61.5	9	0.13-μm CMOS	Rectangular open Loop	2	0.21	-1.5	-2	-9.2

Table 4.2 Comparison of PSi-S-based mm-wave filter with filters implemented in CMOS process

4.8 Conclusion

With the increase in radio applications, the need for electromagnetic spectrum management is still apparent and the front-ends of radio equipment must be equipped with broadband and millimeter band filters, because of the nature of the 5G operating the frequency band ranging from 6 to 100 GHz.

In this chapter, we have dealt with the subject of millimetric bandpass filter. The design of this component does not differ from that used in the centimeter and decimetric bands. However, as we explained, it is a question of mastering the effects of the losses whose impact becomes more important at the millimeter frequencies. These parasitic effects being closely related to the substrate and the technology on which the filter has been implemented, it is a question of retaining the most suitable substrate for the frequency band exploited.

Among the promising substrates for millimetric applications, the standard silicon / porous silicon mixed substrates have excellent insulating properties making it possible to considerably reduce the disturbing effects encountered with other technologies used in the same context.

In order to demonstrate the importance of the link between the performance of the bandpass filter and the millimeter band implementation technology, we have implemented a filter centered at 27 GHz on five different substrates. Then we compared the answers obtained.

We have seen that the implementation on mixed substrate gives more efficient filter, in particular, in terms of loss of insertion, which have been considerably reduced, of reflection losses, which are better, and this on all the considered bands, and finally a noticeable increase in selectivity has been recorded. Consequently, the use of the new substrate has made it possible to increase the performance of the filters in question. Its use in the design of filters can thus open a very promising avenue of research in the 2020 goal of 5G implantation.

General Conclusion

GENERAL CONCLUSION

The structural and nanomechanical properties of porous silicon PSi have studied. The results obtained with different PSi thickness indicate that the porous silicon films obtained on Si wafers with a resistivity of (1-10 Ω.cm) presented interesting results for RFIC (Radio-Frequency Integrated Circuit) for microelectronics applications. Especially for a PSi thickness 50µm where the porosity is around 65% with a high insulating surface area, a surface roughness less than 1 nm and a hardness value (≈1GPa). These values should be advantageous with regard to withstand different devices on top of PSi.

With the foreseen deployment of 5G and *IoT*, the millimetre-wave spectrum becomes highly solicited. Nonetheless, at this specific frequency range the losses due to the silicon-based substrates increase significantly. Thus, to integrate high quality passive circuits, substrates with good insulating properties should be utilized. In this chapter, new variants of porous silicon were introduced. Through accurately controlled fabrication process, very interesting nanocrystalline structure was achieved leading to substrates with good insulating properties, namely, low effective relative permittivity about 3.5 and high effective resistivity values of 5.9 kΩ.cm. The obtained characteristics were emphasized, when compared with three Si-based substrates, i.e., standard silicon, high resistivity silicon, trap-rich HR-Si. Also the reached quality factor of the integrated CPW line was found higher compared to relevant works reported in the state of the art literature. Aiming to demonstrate its usefulness for the integration of mm-wave passive circuit, 27 GHz mm-wave bandpass filter was designed and fabricated on the proposed substrates. The carried out simulations showed that the filter offers better performance, in terms of insertion loss, return losses and selectivity, compared with the same filter implemented in standard resistivity silicon, high-resistivity silicon and other CMOS technologies introduce in the literature. These predicted high performances were validated through the fabrication of the designed filters, and good agreement has been

achieved between simulated and measured data. Therefore, the proposed porous silicon substrate offers low cost alternative to 0.18-µm CMOS technology and trap rich technology, especially when mm-wave circuit design is accounted for. Furthermore, in order to evaluate the impact of temperature variation on the behavior of the designed filter, another series of measurements were conducted, fortunately, the performance of the filters were maintained high demonstrating thus the reliability of the proposed PSi-based substrates.

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Annex

ANNEX A. PROCESS FLOW

1°) Standard cleaning wafer

2°) Metallization back side 200 nm Al

3°) Anodization of Si wafer

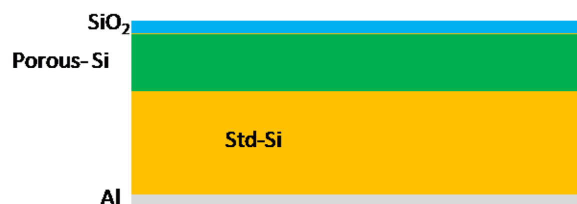
4°) Etching Al back side with H3PO4+Pyrana

5°) Thermal oxidation at 300°C under dry atmosphere of O_2 for 2hours;

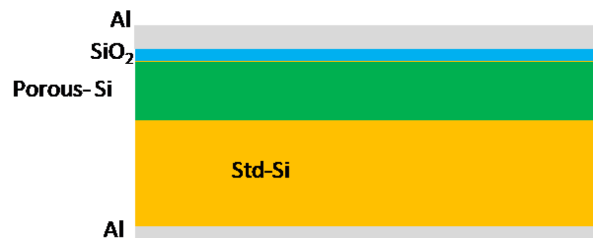
6°) Annealing at 420°Cfor 2 hours in N_2 ambient;

7°) Deposition of 500 nmSiO_2 by Plasma-Enhanced Chemical Vapor Deposition (PECVD)

8°) Metallization back side 200 nm Al



9°) Metallization front side 1 μm Al



10°) Lithography (coating, exposure, develop)

11°) Plasma etching Al

12°) Rinsing and drying.